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This grant to studied and developed innovative methods of hardening electronic systems against the effects of high power microwave (HPM) radiation

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Protection of Electronic Systems from the Effects of High-Power Microwave (HPM) and Ultra-Wideband (UWB) Sources

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Executive Summary

We proposed under this grant to study and develop innovative methods of hardening electronic systems against the effects of high power microwave (HPM) radiation. This research addresses several aspects of the problem as follows:

1. Effective shielding or absorption of HPM radiation at coupling ports and other ingress pathways into electronic enclosures requires an understanding of the statistical nature of electromagnetic fields in complex cavities. The use of metamaterials as high impedance surfaces to mitigate HPM coupling into electronics has been proposed as a possible solution, but HPM coupling mechanisms are not well understood in terms of surface currents at resonant apertures versus other conduction or radiation pathways. "De-Qing" is a method that seeks to reduce the quality factor of electromagnetic cavity modes, but the HPM field distributions in cavities may be focused by chaotic scattering into localized hot spots that are not effectively mitigated by lossy materials. Therefore a detailed study of the statistics of HPM coupling, cavity field distributions and ingress were conducted. The results show that the statistics of HPM coupling to circuits in complex cavities obeys the Rayleigh distribution in moderately reverberant enclosures over long (> 10 propagation round-trips) time scales, but are Rician distributed over shorter time scales. The results give a solid basis for predicting localized HPM field intensities in cavities and the HPM voltages they induce in circuits. This capability provides a foundation for designing physical (material) HPM mitigation for generalized cavity shapes for all types (e.g. pulse modulated, UWB or damped sinusoid) of HPM waveforms.
2. A study of basic effects mechanisms and mitigation in communications electronics using photonic optical interconnects (OI) for digital communications channels and digital differential signaling was conducted. These concepts involves breaking the direct conductive path between the data bus and receiver or mitigating the HPM-induced common-mode voltage on the bus, respectively. Thus logic state of the core CMOS devices operate in an environment that is electrically isolated from HPM radiation. Tests on advanced COTS low-voltage differential signaling (LVDS) and single-ended (SE) data busses were conducted and compared to circuits that we designed and fabricated. The measured coupling parameters and HPM rejection ratio were shown to be at least 17 dB higher than SE CMOS based on the same process parameters. The tests were performed using an advanced chaotic HPM source designed to stress the system under test and simulate worst-case HPM conditions.

Introduction: The threat to electronic systems from high power microwave (HPM) sources has motivated studies of the basic electronic mechanisms that operate in circuits to render them susceptible to upset and damage. Empirical effects testing on complete electronic platforms have shown that HPM radiation couples into electronics via many ingress pathways such as power and interface cabling, cooling vents, joints in enclosure panels, etc. HPM radiation may cause permanent damage to gate insulators or a variety of nondestructive, persistent failures which are collectively classified as "system upset" [1]. While radiation tests yield important information about the susceptibility of a given system to a particular HPM excitation, it is often difficult to trace upset to individual components or subsystems. Previous studies of HPM and EMP effects on integrated circuits (IC) in [2]-[9] have shown that a variety of mechanisms may upset circuits. Rectification of radio frequency (RF) radiation by semiconductor devices was reported in [3]-[6] wherein effects were related to low frequency voltages produced by the demodulation of the HPM carrier by semiconductor devices. In [2] this process was shown to cause bias shifts in discrete bipolar devices and logic errors in CMOS digital circuits in [3]-[6]. Generally, in earlier work it was

concluded that susceptibility decreases monotonically for frequencies above ~200 MHz due to the capacitive loading of semiconductor junctions at device inputs. While this conclusion may have been valid for yesterday's micron-scale IC's, advanced systems based on sub-micron devices require very high input impedances to enable high data transmission rates [10]. The secondary effect of such high impedances is to increase the frequency range of HPM effects. This high-impedance requirement has driven revolutionary advances in devices, electronic packaging and electrostatic discharge (ESD) protection technologies [11], but the HPM susceptibility of modern circuits has evolved as a consequence. Tests on more recent CMOS technology support this hypothesis [12], [13]. In this work, we present the results from an experimental and analytical study aimed at characterizing the input response of CMOS integrated circuits to pulsed microwave excitation at frequencies up to 4 GHz. We focus on the effect of signal voltages induced by HPM fields that couple onto printed circuit board traces. Methodologies for quantifying this type of coupling has been investigated in literature, for instance in [29] and [30]. A calculation of circuit trace signals associated with the coupling of incident electric field strengths above this magnitude is given in [32]. The goal of this characterization is to understand, with a device physics foundation, the elementary HPM interaction with the ESD protection devices. We are primarily interested in understanding the impact on the input terminal voltages when ESD protection devices are driven into nonlinearity. This also includes studying how junction capacitances inherent to these common ESD protection devices combine with the parasitic impedances of packaging elements and printed circuit board traces to yield resonant structures at circuit inputs. Results from previous work have suggested that HPM signals can interact with these resonant structures to produce voltages capable of driving undesirable circuit responses and potentially system upset [14]. Our results verify this, as well as provide an analysis of the underlying mechanisms.

Significance of Research: Improving the understanding of the physical mechanisms underlying HPM effects will lead to more effective evaluation of system susceptibility. Critical vulnerabilities in systems could be identified in individual components if accurate modeling capabilities are developed. Improved prediction capabilities for HPM effects also benefits the development of mitigation strategies designed to address specific critical vulnerabilities. For this reason, we also examine the capability of the Berkeley Short-channel IGFET Model (BSIM) to accurately predict response voltages generated at device input terminals. Based on the analysis of the underlying device physics of the ESD protection circuits, we present a strategy which modifies existing scalable CMOS BSIM compact model parameters to improve simulation accuracy of high frequency ESD device response. We characterize effects in test circuits designed in-house and analyze the nonlinear behavior of ESD protection devices. Generic CMOS ICs were designed and fabricated as test circuits according to standard COTS logic functions and VLSI layout design rules. The details of our experimental method and measurement results are reported since there are no standardized methods prescribed for HPM effects testing. Observations include increases in the DC voltage level at the input caused by the interaction of microwave pulses coupled to ESD protection circuits on CMOS integrated circuits. We characterize resonances due to the parasitic reactance of IC packaging and chip metalization and how they contribute to the overall voltage response. We also report the results of a new method of modeling HPM effects in CMOS using a substrate network that correctly calculates the non-quasistatic (NQS) response of the ESD.

A. Typical Digital Circuit Input Stage Construction and Observed Effects

The input stage of a digital circuit consists of the MOSFET gates of an input stage buffer, preceded by ESD protection devices. One typical implementation uses diode-connected MOSFET structures [19], in the configuration shown in Fig. 1. ESD action occurs when the gate-grounded NMOS (ggNMOS) or the gate-coupled PMOS (gcPMOS) receive input voltages that are below ground or above Vdd by at least a forward diode drop, respectively. When HPM couples to the input of a digital circuit, three effects are observed:

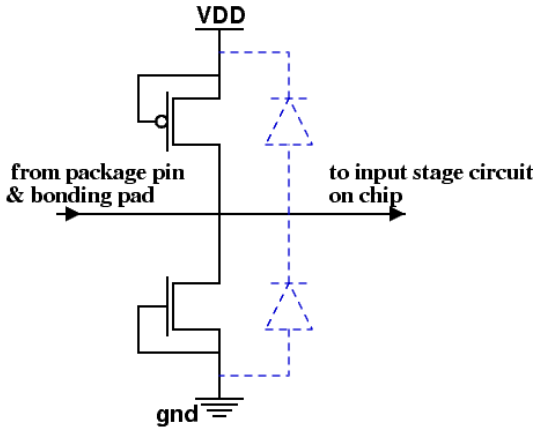

Fig. 1. A typical implementation of ESD protection circuitry at an input pin for a CMOS IC.

1. The HPM signal can cause a DC voltage offset shift at the pin through the following mechanism. The incoming HPM

voltage is superposed on the logic level that may be present on the data bus, and the ESD devices are driven into nonlinear operation. The diode response depends on the HPM frequency and are also unequal for the NMOS ESD device and the PMOS ESD device, leading to a detected DC voltage at the pin. In this work, we refer to the junction operation in the quasi-static regime as "rectification" and the non-quasi-static regime at higher frequencies as "detection" behavior. In the remainder of this section, we analyze the responses of the NMOS and PMOS devices that will lead to the characteristics of the measurement results we will present later in the paper.

2. The average current drawn from the rail (V_{DD}) node may increase as a result of the extra DC "biasing," as per the previous effect.

3. Both of these aforementioned effects plus possible direct coupling through the chip structures may cause errors at the output, including bias shifts, as well. For this particular work, we will not focus on the latter two effects in any detail.

B. NQS Regime Behavior of ESD Protection Devices

Here we examine the rectification action and the transient responses of the PN junction associated with the ESD protection devices, in order to identify the underlying cause of the behavior described above and demonstrated in Section III. The significant PN junction sin this case are the p+/n drain-body junction of the gcPMOS and the n+/p drain-body junction of the ggNMOS, whose behavior determines the ESD structure response to the RF input [13].

Figure 2 shows the measured IV curves for the ESD protection devices in our test implementation, with the voltage signal applied to the input pin and the current going into the pin measured. More details about the physical design of this implementation are given in Section III. As we will analyze in the rest of this section, at higher frequencies and injected power levels, the diode response deviates from the ideal, as the devices enter a non-quasi-static (NQS) operation regime. Further characterization of the response of these devices by themselves to RF injection, including information about their current draw, can be found in [17]. One point to note is that the current draw of these devices, even during the most intense HPM excitation conditions we have emulated in our setup, stay well below the level of an amp. The typical current levels observed in [17], while measured with a 50 Ω in series with the diode, do not go beyond 5 mA at low frequency with the excitation level at 15 dBm. The level naturally falls off with higher frequency. Therefore, the effects we report here are distinct from the usual effects of electrostatic discharge events, such as diodes entering the snapback regime or the indirect mechanism of bit-error creation through power injection into the on-chip power distribution network system.

At higher RF frequencies, the difference between the transient responses of the two ESD device types present in the implementation shown in Fig. 1 changes the detected voltage levels. Diode transients are governed by the rate of change in the minority carrier concentration with respect to time. An important characterization parameter is the "reverse recovery time": The time for excess minority carriers to transit away from the junction boundary and recombine after a switch from forward to reverse bias. This time constant determines how rapidly a diode can switch and thus governs the frequency response of the device. If the reverse recovery time is very small compared to the period of an RF input, the diode will behave ideally, rectifying the RF signal. Under this condition, called the quasi-static regime, the junction will conduct for half the RF period. As the period of the RF signal approaches the reverse recovery time, the diode will conduct for more than half the period and the rectification efficiency of the diode diminishes. This is referred to as the non-quasi-static regime.

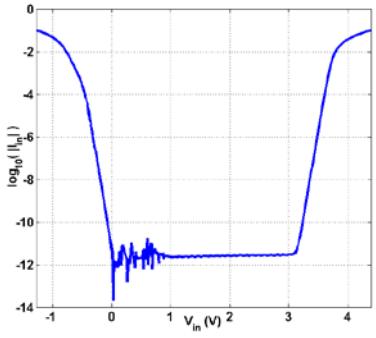

Fig. 2. Measured IV curves at an input pin of our test circuit due to the presence of the ESD protection devices demonstrating their diode behavior. The chip is powered (ground and V_{DD} = 3V connected) and the voltage is applied to an input pin, and the current going into the input pin is measured. Below 0 V (ground level), the ggNMOS is conducting. Above 3 V (V_{DD}), the gcPMOS turns on. In the linear parts of the log(I_d) vs. V curve, the NMOS section has a slope of magnitude 16.41 while the PMOS-section slope is 15.89.

The diffusion of minority carriers away from the PN junction boundary is described by the time-dependent diffusion equation [21]-[24]:

$$\frac{\partial n_p(x,t)}{\partial t} = D_n \frac{\partial^2 n_p(x,t)}{\partial x^2} + \frac{n_p(x,t) - n_{p0}}{\tau_n} \quad (1)$$

$n_p(x,t)$ is the minority carrier concentration as a function of position and time, n_{p0} is the zero-bias minority carrier concentration, D_n is the diffusion constant, and τ_n is the minority carrier lifetime. In ESD protection devices, the distance from the drain-body junction to the source is much shorter than the diffusion length and the minority carriers will be swept away by the source-body built-in junction before they can recombine in the bulk. This is essentially a short-base diode for which Kingston presents the analytical solution for Eqn. 1 in [22]. Assuming that the ratio of the forward-bias current to the reverse current during the recovery is 1, Kingston's results show that the reverse recovery time is approximately $0.5\tau_{eff}$, where τ_{eff} is the minority carrier lifetime [22] given by Eqn. 2:

TABLE I
MINORITY CARRIER DIFFUSION CONSTANTS IN SILICON

Minority carrier	*Diffusion Constant* (cm^2s^{-1})	τ_{eff} (ps)
Electrons	34.6	234

$$\tau_{eff} = \frac{L_{eff}^{\ 2}}{D_{n,p}} \qquad (2)$$

The effective diffusion length, L_{eff}, is the distance from drain-body PN junction to the source, which for our devices is 0.9 µm. The diffusion constants $D_{n,p}$ are defined by Eqn. (3):

$$D_{n,p} = \frac{kT}{q}\mu_{n,p} \qquad (3)$$

k is Boltzmann's constant, T is the temperature, and $\mu_{n,p}$ are the silicon electron or hole mobilities respectively. The common values of $D_{n,p}$ for electrons and holes in silicon and the calculated effective minority carrier lifetimes are given in Table 1 [25]. Table 1 can be used to calculate the reverse recovery time using Kingston's results, with which we can then estimate the ESD protection devices' average current versus frequency for sinusoidal excitation. Here it is assumed that the drain-to-body diode remains conducting throughout the reverse recovery time, when actually the conductivity would change as the minority carrier concentration at the junction boundary drops. However, this approximation is adequate for estimating the diode behavior as a function of frequency using the following method: We compare the reverse recovery time to the total period of a sinusoidal signal being applied as the input. As the frequency increases, the reverse recovery time takes an increasingly higher portion of the half-period when the diode should have turned off. This would reduce the DC level "detected" out of the RF signal across a load impedance.

Using this method, in Figure 3 we show the normalized average current responses vs. frequency for an arbitrary load with a sinusoidal signal as the excitation. Note that the frequency response of the PMOS device rolls off at a lower frequency than that of the NMOS. This will be shown to be consistent with the measurements presented in Section III. At high enough frequencies where the PMOS and NMOS responses are appreciably different, the average DC voltage in the signal line to which they are both connected rises above $V_{dd}/2$ with increasing input signal amplitude, whereas in the frequency range where the diodes are in quasi-static behavior and balance each other, this average levels off at nearly $V_{dd}/2$.

The physical reason for the differing behaviors of the two ESD protection devices lies in the different minority carrier mobilities. As described above, the drain/body junctions of the NMOS and PMOS ESD protection devices are asymmetric diodes (n+/p and p+/n, respectively). Therefore, for the NMOS (PMOS) device, the minority electron (hole) concentration in the bulk will govern the diode transients. The electron mobility in silicon is generally higher than the hole mobility, accounting for the difference in the diffusion constants in Table 1. As a result, the transit time from the drain/body diode depletion region boundary to the source contact for a hole in the PMOS ESD device is longer than the same for an electron in the NMOS device, which results in a longer reverse recovery time and thus the earlier roll-off in the frequency response.

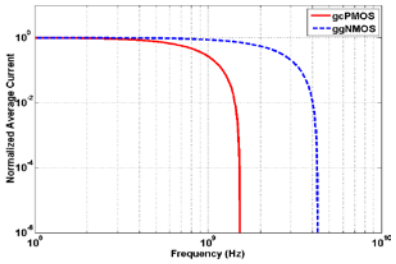

Fig. 3. Normalized average current response of the ESD protection configuration transistors to sinusoidal excitation as a function of frequency.

II. TEST CIRCUIT DESIGN AND EXPERIMENTAL RESULTS

A. Test Circuit Design and Basic Characterization

Previous efforts to characterize and model HPM effects in circuits and devices involved experimental evaluations of commercial devices and the use of either basic spice models or models provided by the manufacturer [14], [15]. The process-specific device parameters and circuit topologies are generally not made publicly available. This

presents limitations to HPM effect modeling efforts on commercial, off-the-shelf devices.

In order to avoid these restrictions, a representative CMOS integrated circuit (IC) was fabricated for this work.

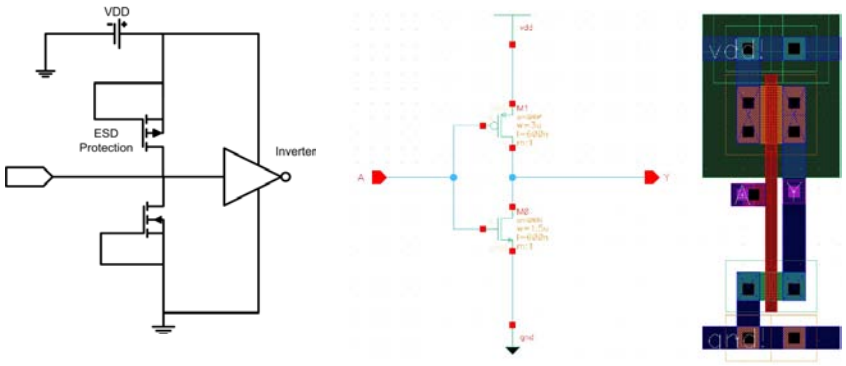

Fig. 4. Schematic of the test IC fabricated on the ON Semiconductor 0.6 µm process technology (left). The test circuit consists of ggNMOS and gcPMOS ESD protection devices followed by a buffer circuit, the first stage of which is an inverter. The inverter schematic is given in the middle, and the layout on the right.

The IC was designed using the Cadence Virtuoso layout tools and fabricated on the On Semiconductor (formerly AMI) 0.6 µm process, available through the MOSIS service [16]. A schematic of the particular circuit we tested is shown in Figure 4, along with a layout for the full integrated circuit. The chip dimensions are 1500 µm x 1500 µm, with bonding pads 80 µm on a side. The chip is packaged in a ceramic leaded-chip-carrier package, LCC44 by Kyocera, which has a 0.76 cm cavity size. The bonding wires, therefore, have a parasitic inductance of approximately 4 nH.

The test circuit was designed to correspond to the input of a typical commercial IC, which consists of ESD protection devices followed by an input buffer. ESD protection devices are ubiquitous devices vital to the IC industry. They are designed to prevent IC failure due to electrostatic discharge events at device terminals during the IC production and operation [17], [18]. Electrostatic discharges are short-duration events with peak currents reaching tens of amps and voltages reaching tens of kV. If an ESD event occurs, the protection devices provide a low-impedance path to ground for high peak currents and clamp the terminal voltages to a safe level. As mentioned previously, the ESD protection configuration used in the test circuits is the ggNMOS/gcPMOS pair [19]. The physical dimensions of these devices are large compared to the transistors that make up the core logic. In our implementation, each device consists of 12 fingers. The dimensional parameters are provided by Table 2.

The grounded gate (or connected to V_{dd} for the gcPMOS) creates diodes between the input terminal and both V_{dd} and ground, both with relatively large drain-body PN junctions. During normal digital input excitation, both PN junctions remain in reverse bias, and the operation of the functional circuit in the IC is unaffected by the presence of these devices other than the loading due to the junction capacitance.

The input buffer circuits accept the input signal to the IC and convert it to a clean signal for the functional logic circuits. There are several common input buffer circuits found in literature [20]. Common to all is the high input impedance characteristic of MOS technology. For this reason our implementation has an inverter to represent the input stage of this buffer. The dimensional parameters of the inverter are presented in Table 3.

The test circuit was packaged in a LCC44 surface mount carrier and soldered to a printed circuit board (PCB) designed and fabricated for these measurements. All ground connections to the

TABLE II
PHYSICAL PARAMETERS OF THE ESD PROTECTION DEVICES

Gate Width (µm)	30
Gate Length (µm)	0.9
Drain Diffusion Area (m^2)	1.845e-10
Drain Diffusion Perimeter (µm)	72.6

TABLE III
PHYSICAL PARAMETERS OF THE INVERTER CIRCUIT NMOS AND PMOS

NMOS, Gate Width (µm)	7.95
NMOS, Gate Length (µm)	0.6
NMOS, Drain/Source Diffusion Area (m^2)	7.16e-10
NMOS, Drain/Source Diffusion Perimeter (µm)	113.4
PMOS, Gate Width (µm)	15.6
PMOS, Gate Length (µm)	0.6

test chip occur through vias to a metal backplane. The power connection to the circuit is made through an SMA connection at the edge of the board which connects to the circuit through a short trace. A 0.1 µF local bypass capacitor is connected between the power trace and ground through a via positioned closely to the test chip power pin. The input and output signal traces are 0.6 mm wide and trace lengths range from 1 cm to 3 cm. The input trace has a surface mount 10 kΩ pull down resistor connected in parallel to the input t erminal. The parasitic impedances

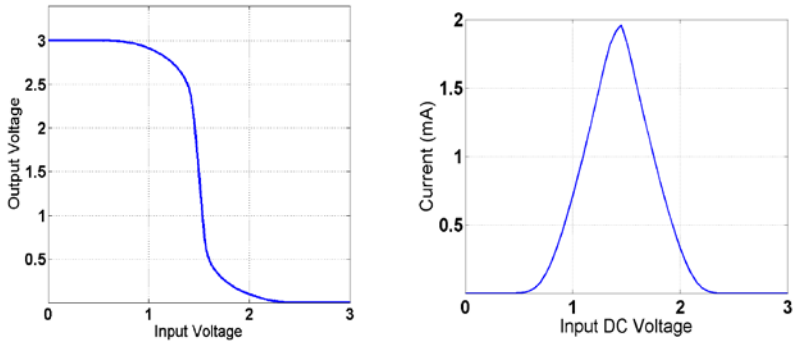

Fig. 5. Voltage and current transfer curves of the test inverter circuit in normal operation.

introduced by the circuit board traces were desirable in that they provide a realistic representation of common circuit boards, which will have an impact on terminal voltages produced by HPM excitation.

We first present the basic characterization of our circuit, to demonstrate normal operation. Figure 5 gives the inverter voltage and current transfer curves (V_{out} vs. V_{in} and I_D vs. V_{in}).

B. RF Injection Experiment Setup and Methodology

A schematic of the experimental setup to observe the effects of RF injection into the input pin of our test circuit is shown in Figure 6. An Agilent E8257D analog signal generator is used to generate pulse modulated HPM signals. These signals are directed through an RF amplifier in order to raise the power output capability. A 100 MHz high-pass filter is placed in the signal line to block any spurious DC voltage from the amplifier output. The RF signal is delivered to the input PCB trace through a Cascade Microtech FPC-1000 ground-signal-ground (GSG) probe. GSG pads were fabricated at the ends of the input and output traces to match the RF probes.

Figure 7 shows photographs of the experimental setup. A bias tee is used to measure the detected DC voltage at the test circuit input. In general, no DC bias is applied to the input terminal during measurements, and there is no DC offset present in the injected RF signal. Therefore any DC voltage offset detected through the bias tee is due to the circuit response to the HPM signal. Electronic instruments, such as the RF source and the oscilloscopes, were connected to a central control computer through a GPIB bus. The front panel control of each instrument was managed with a virtual instrument created using the Agilent VEE Pro platform. The experiment was conducted by injecting a signal generated by the RF source, which represents an HPM signal that would potentially couple into a signal trace of a conventional electronic system, into the test circuit input trace. The work in [32] verifies that the amplitude of the injected signals are consistent with the signal that would arise from the coupling of HPM fields into PCB traces.

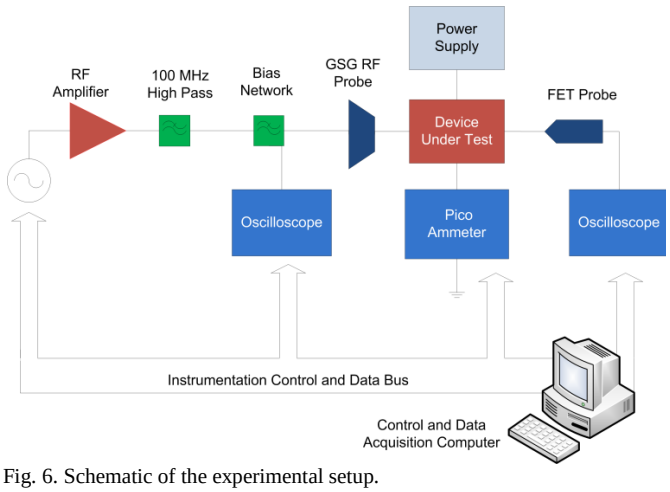

Fig. 6. Schematic of the experimental setup.

Typical HPM sources are pulsed sources with operating regimes on the order of nanoseconds to microseconds. Therefore, the input signal was pulse modulated in order to replicate a more realistic HPM scenario and to prevent thermal effects in the DUT from dominating the measured data. The modulation pulse width was set to 7 µs and the repetition period was 100 ms. The fall and rise times of the modulation are 10 and 23 ns, respectively. The output power from the RF amplifier was stepped from -20 dBm to 20 dBm and the frequency was stepped from 100 MHz to 4 GHz in increments of 100 MHz. Figure 8 shows the

normalized spectrum of an example of this excitation pulse, taken before the amplifier with 1 GHz frequency and 0 dBm amplitude. The detected voltage measured through the bias tee was calculated as the cycle mean of the voltage waveform recorded for each frequency and power setting using

$$V_{\text{det}} = \frac{1}{\tau}\int_{\tau} v(t)dt \quad . \quad (4)$$

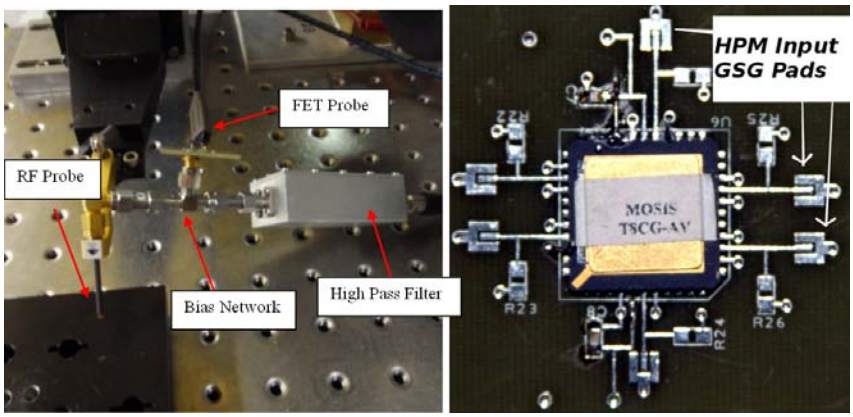

Fig. 7. Left: The setup to inject HPM excitation into the pins of the circuits under test and measure the resulting signal at the pin. The HPM excitation enters through the high-pass filter and the bias network allows the monitoring of the signal levels at the pin, which is contacted through the RF probe. Right: A typical PCB design used in these experiments. The ground-signal-ground (GSG) probe pads are used with the RF probe depicted to the left to inject the HPM excitation.

Here, V_{det} is the detected DC voltage, $v(t)$ is the waveform measured at the bias tee and τ is the period of one RF cycle. Figure 9 shows an example input waveform and the corresponding V_{det} recorded by the oscilloscope for a carrier frequency of 400 MHz and power level of 16 dBm. The dashed red line shows V_{det} vs. time after (4) is applied to the measurement data. All the detected DC voltage levels, giving the measured input response of the test circuit throughout the full input power and frequency ranges, are collected into a contour plot at Fig. 10. The x-axis is the HPM frequency, the y-axis is the input power to the circuit, and the contour levels represent the detected DC values at the input pin. There are several interesting features to the response demonstrated in this plot. The first feature in question is the occurrence of peaks and valleys in the measured response voltage, especially at higher frequencies. In order to explain these, consider the plot in Figure 11, which gives the measured s-parameters of the input signal traces of the test circuit. The s-parameter measurement reveals the resonance due to the parasitic impedances along the input path. Notice the strong resonance between approximately 1.4 and 1.9 GHz. Within this frequency band, less than 10% of the HPM excitation is transmitted to the circuit, which is consistent with the severe drop-off in the input voltage response over the same frequency range in Fig. 10.

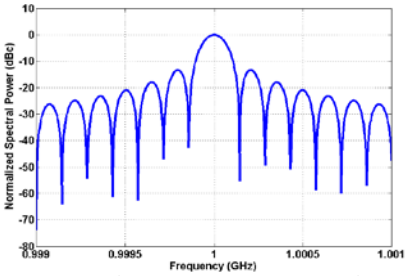

Fig. 8. The spectral power of an HPM excitation pulse, for an example pulse with 1 GHZ frequency and 0 dBm amplitude, with 7 µs pulse width and 100 ms pulse period as used throughout this work. Spectral power referenced to the carrier power.

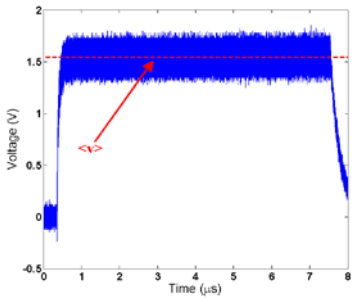

Fig. 9. The measured input waveform at the input pin to the inverter circuit with the ESD protection devices. The input pin is not biased with a DC level. The injected HPM pulse starts at approximately 0.25 µs and lasts for 7 µs. When this pulse arrives, the response of the ESD protection devices causes the DC shift at the pin, which is marked as the detected voltage level $<v>=V_{det}$ in the figure with the dashed line.

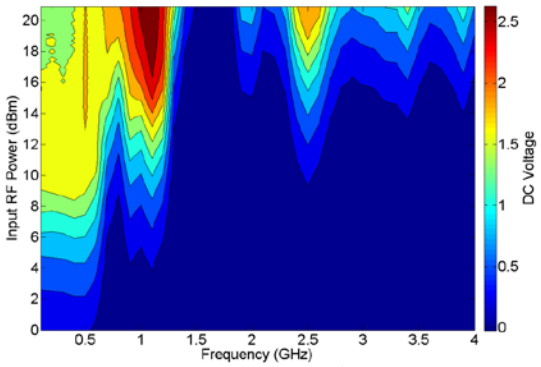

Fig. 10. Detected DC levels at the input of the test circuit under HPM excitation. Note that the example data point shown in Fig. 9, collected at 0.4 GHz and 16 dBm, matches its level in this plot as slightly above 1.5 V.

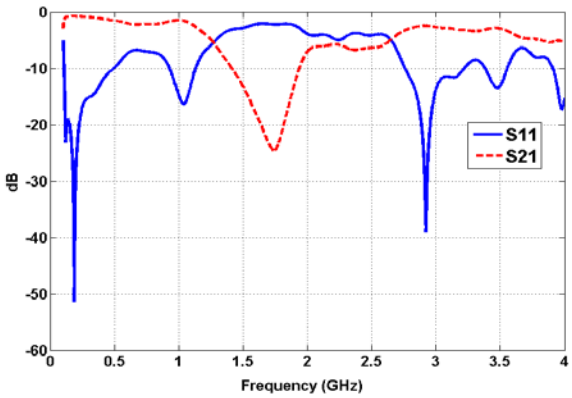

Fig. 11. Measured S parameters for the input circuit board trace of the DUT.

The second interesting feature is the variation of the peak input response voltage with frequency. The response voltage increases uniformly for frequencies from 100 MHz to 500 MHz until it plateaus at slightly above 1.5 V. This can be seen more clearly in Figure 12, which shows cross-sections taken from Fig. 9 across the power axis at four excitation frequencies, displaying the detected DC voltage across the input amplitude range at 200, 600, 700 and 800 MHz. To explain this behavior, we recall the analysis presented in Section II. At lower frequencies, the results resemble what one would expect if the ESD protection devices were treated as ideal diodes. At RF amplitudes above the diode turn-on voltage, the ggNMOS device rectifies the RF signal, and the mean voltage at the input node increases with the amplitude. Once the mean voltage plus the RF signal amplitude rises above V_{dd}, the gcPMOS will also turn on during the appropriate half of the HPM excitation period, which counterbalances the effect of the ggNMOS. As a result the response voltage should plateau at V_{dd} /2, which is close to the behavior shown in Fig. 11 for the 200 and 600 MHz input frequencies. But at higher frequencies, the gcPMOS response rolls off, reducing its detected DC voltage further and making it unable to match that of the ggNMOS, which allows the response voltage to rise above V_{dd}/2 as observed. To ensure that the responses of the in-house designed test circuits are consistent with the typical responses of commercial off-the-shelf CMOS devices, these experimental results were compared to the input response of a commercial, off-the-shelf inverter integrated circuit. This inverter was operated at V_{dd}=3.3 V. Figure 13 shows the input DC response measurement results.

Between approximately 200 and 500 MHz, the voltage also rises above V_{dd} /2 as the input HPM power increases beyond 10 dBm, as was observed in our own test circuit at frequencies above 600 MHz. Also, resonant behavior, such as the large dip in the response at 600 MHz, resembled those observed in the custom test circuits as well. However, for the commercial device this behavior shows up at a lower frequency than for the custom test circuit. This is likely due to the difference in the process technology and parasitics of the packaging and the printed circuit board.

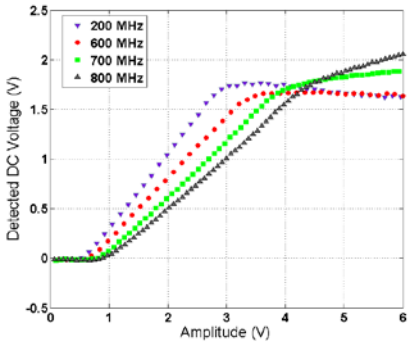

Fig. 12. Detected DC voltage vs. injection amplitude at 200, 600, 700 and 800 MHz. These lines are cross-sections taken from Fig. 10 across the power injection axis at four frequency points. At the lower frequencies, the response "saturates" at slightly above V_{DD}/2, whereas at higher frequencies it continues to rise with higher input power. As explained in the text, this is caused by the gcPMOS being unable to "match" the rectification response of the ggNMOS.

III. Modeling

Since we have shown that ESD protection devices play a significant role in HPM effects, accurate modeling of these devices is critical to effective prediction efforts for such effects. This section discusses a preliminary modeling technique to improve simulation accuracy of PN-junction-based ESD protection devices. Simulations were performed using Agilent Advanced Design System (ADS), with the transient and harmonic balance techniques, and the Berkeley Short-channel IGFET Model (BSIM) version 3.1 or 4.5. Test wafer extraction of the BSIM compact model parameters were provided by the semiconductor foundry which fabricated the test circuits. The harmonic balance technique was used for its advantage in speed,

although the user always has to be mindful that it performs calculations only at the harmonics of a set drive frequency. Our simulations were set up to go up to the 8th harmonic. Transient simulations are more accurate for signals with multiple frequency components, large signals, and where nonlinearity may be present or dominant. However, they take much longer to perform, as many periods may be necessary under nonlinearity or large signal conditions for the results to reach steady state.

Although BSIM is excellent at accounting for short channel effects that become increasingly substantial as device dimensions continue to scale smaller, it does not accurately model the drain-body PN junction, especially under forward bias conditions [26]. Specifically, BSIM 3v1 models do not account for diffusion charge due to minority carrier concentration and therefore cannot model diode transients completely for this particular junction. Although BSIM transistor equations do calculate the junction capacitance, they do not accurately model the diffusion capacitance when this junction is in forward bias, which increases the total capacitance substantially [26].

Figure 14 is a plot of the input response with an excitation frequency of 2.5 GHz as measured by the experiment and predicted by simulation. The simulation is performed strictly using BSIM model parameters as provided by the foundry. There are two key differences between the measurements of the detected DC voltage and those predicted by the simulation. The rectification efficiency predicted by simulation is greater than the actual rectification efficiency at this frequency. Also, the simulated response voltage plateaus at approximately $V_{dd}/2$, whereas the measured response increases beyond this value. Both of these discrepancies are related to the lack of adequate modeling of diode transients provided by BSIM.

It is possible to emulate the effect of the reverse recovery time differences between the ggNMOS and the gcPMOS as described in Section II by making use of the substrate resistance network model available in BSIM4 [28]. Designed for more accurate high speed/RF simulation, the substrate resistance network introduces virtual nodes within the transistor near the drain/body junction, the source/body junction, the channel midpoint, and the body contact; these nodes are then connected with resistors. Figure 15 shows a schematic of this network.

In the normal course of using BSIM, the resistance values for this network should be extracted from measurement data from the transistor in question. In our problem, this resistance network is used to provide a time constant along with the junction capacitance of the drain-to-body diode, and this time constant can be tuned to compensate for the reverse recovery time of the diode for each of the ESD protection devices. Since BSIM models the voltage-dependent junction capacitance for the drain/body and source/body junctions, but does not model the forward bias diffusion capacitance for the drain/body contact in detail, in order to compensate for the full time constant of this junction during the turn-off we have to use resistance values somewhat larger than the expected value of the equivalent series resistance for this diode (which can be obtained either by measurement or with an approximate calculation including the doping-dependent substrate resistivity). This allows us to observe, by simulation, results that better match trends observed by measurement. For instance, in Figure 2 we had presented the IV curves looking into an input pin of our custom test circuit and scanning the DC bias at this pin between -1 and 4 V. Figure 16 shows results of simulating this particular measurement with and without the substrate network option in place. The resistance values used in the substrate network in this simulation are 125 Ω for the gcPMOS and 75 Ω for the ggNMOS. Note that the current is unreasonably high for the simulation if the substrate resistance network is not included, while the simulation *with* the substrate resistance network gives a reasonably good match with measurement.

Figure 17 shows the results of the detected DC response simulation at 2.5 GHz with the substrate resistance network included. This inclusion improves the simulation result accuracy greatly, as can be seen in

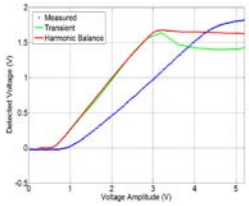

Fig. 14. Comparison of the measurements of the detected DC response at an excitation frequency of 2.5 GHz with simulation results obtained using BSIM parameters provided by the foundry.

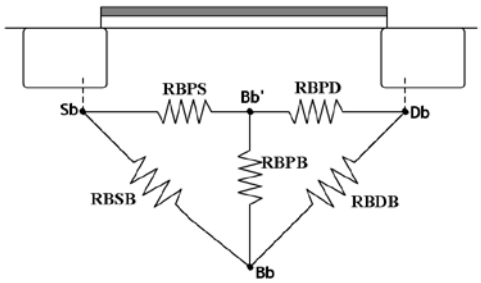

Fig. 15. The substrate resistance network included in BSIM4 (adapted from [28]).

comparison to Figure 14. As mentioned above, the resistance values to be introduced into the gcPMOS device have to be higher than those introduced into the ggNMOS device to match measurement results, which is consistent with our interpretation of the difference in device behavior described in Section I

The second important factor to consider when modeling circuit operation with simulation is the parasitic elements present in the measurement setup, including board traces and connections. With the ADS feature which allows the user to introduce the measured s-parameters of a setup as a one-port or two-port element, we can include the s-parameters of the input trace and connections, which were presented in Fig. 10, in our simulation. Figure 18 shows simulation versus measurement results for a fixed input power of 15 dBm over the entire experimental frequency range, the simulation including both the substrate resistance network and the measured parasitic impedances from the experimental setup. These simulation results show good agreement with experimental measurements. The most noticeable deviation, in the range of 0.1 to 1.3 GHz, is approximately 15%.

Optical Interconnects

As CMOS integrated circuits continue to achieve smaller feature sizes in the nanoscale, interconnection is becoming the main bottleneck for improved device performance. The majority of size and engineering effort to date is dedicated to increasing interconnect densities and reducing power dissipation. Optical interconnects hold tremendous promise for overcoming many of the limitations of conventional electrical interconnects by providing greater bandwidth and lower power dissipation. Another potential advantage of optical interconnects is that they hold great promise for engineering integrated circuit devices that are less sensitive to interference by high power microwave (HPM) signals. Such signals could arise naturally from nearby high power transmitters such as cell phone towers, and could also be intentionally introduced as a method to disrupt the operation of critical hardware. For integrated circuits performing critical operations it is crucial to develop methods that are robust against such potential interference. Optical interconnections can provide a unique solution to this problem. It is now understood that the majority of interference from background microwave sources feeds into CMOS chips through capacitive and inductive coupling with interconnects that connect the integrated circuit (IC) to the rest of the system. By replacing these electrical connections with all optical interconnects an IC can be completely isolated from the external microwave environment, providing a highly robust circuit for critical applications.

In this project, we will develop and study integrated photonic waveguides as a tool for creating HPM robust circuits. Such interconnects must be engineered in a material system that is compatible with CMOS devices. Silicon Nitride (SiN) integrated photonics are ideally suited for this application because they are highly insulating and are fully compatible with silicon CMOS fabrication. We will engineer optical interconnects based on SiN photonic waveguides. Fabrication and optical characterization of the optical interconnections will be carried out by the research group of Edo Waks. Their research group has extensive experience in design, fabrication, and optical characterization of integrated photonic devices. Characterization of the HPM response of these devices will be carried out by the research group of John Rodgers, who have extensive experience in HPM generation and characterization. The specific project tasks we will carry out are listed below:

1. Development of SiN optical interconnects on silicon and silicon dioxide substrates.
2. Demonstration of electrical to optical transduction and detection over an optical channel.
3. Characterization of device performance under HPM irradiation
4. Develop methods for scaling to complex IC circuits via integrated photonic design

The University of Maryland provides an ideal environment for this joint project. The Waks group is fully equipped with optical characterization tools needed to study the performance of high bandwidth optical interconnects. The Rodgers lab is fully equipped with microwave generation and detection tools needed to characterize the device performance. In addition, the Maryland Nanocenter provides a full range of

A Research Effort

A.1 CMOS Integration and Photonic Guard Rings

One of the main advantages of developing SiN integrated photonic devices is that they can be easily incorporated into CMOS chips to create hybrid photonic and electronic processors. An example of how this can be done is illustrated in Fig. 1. A planar CMOS chip, such as the one shown on the left image, can be capped with a thin layer of insulating SiO_2. SiN can the be deposited on top to form the substrate for the photonic devices. Once this is accomplished ebeam patterning can be used to create ridge waveguides, microdisk cavities, and photonic crystals. These device structures can all be naturally integrated, and QDs can be incorporated into the center of the structures using previously describe technique, or deposited on the surface in conjugated polymers for electrical injection.

The integration of CMOS devices with photonic overlays has a broad range of applications. Photonic channels can offer significantly improved bus speeds, and provide an additional dimension over which interconnections can occur. It has been argued that such interconnections could lead to significant design simplifications of CMOS devices, provide methods for *crossing wires*, enable convenient clock distribution, and lead to reduced power dissipation [1].

Our research will focus on methods to incorporate the integrated optical devices that we are developing with CMOS to achieve improved device performance. One of the main applications that we currently target is the development of optical guard rings in CMOS chips. There is currently tremendous interest in the Air Force for methods to defeat electronics with high power microwave (HPM) signals, as well as to protect electronic components from enemy attack by HPM signals [2–5]. Methods to isolate CMOS devices electrically from external influence could significantly improve the robustness of devices to HPM attacks.

We propose a method to use photonic channels to isolate CMOS devices for protection to HPM, which should significantly improve their robustness in the field. The idea is illus-

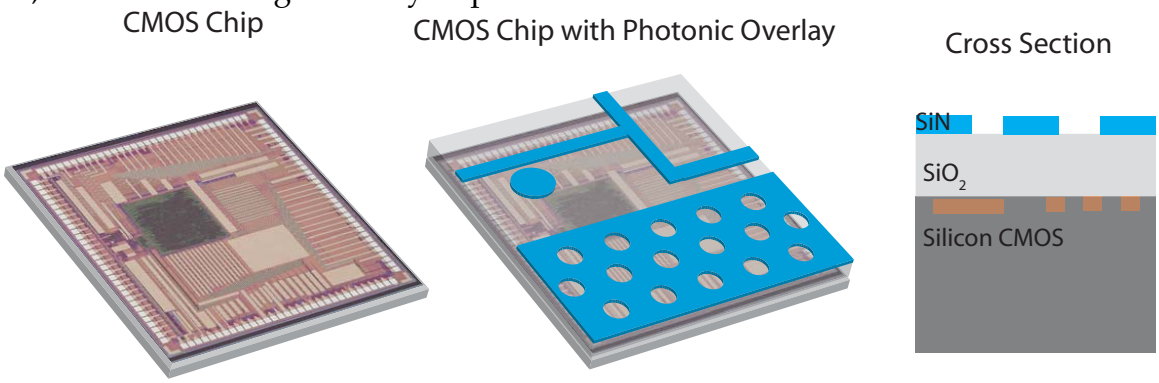

Figure 1: Illustration of technique for integration of cmos structures with integrated photonic devices. The bare cmos device, shown on left, is capped with an insulating SiO_2 insulating layer. SiN is deposited on top of the insulating layer and patterned to form optical waveguides, microdisk resonators, or photonic crystals. The right image shows a cross-sectional view of the proposed device structure.

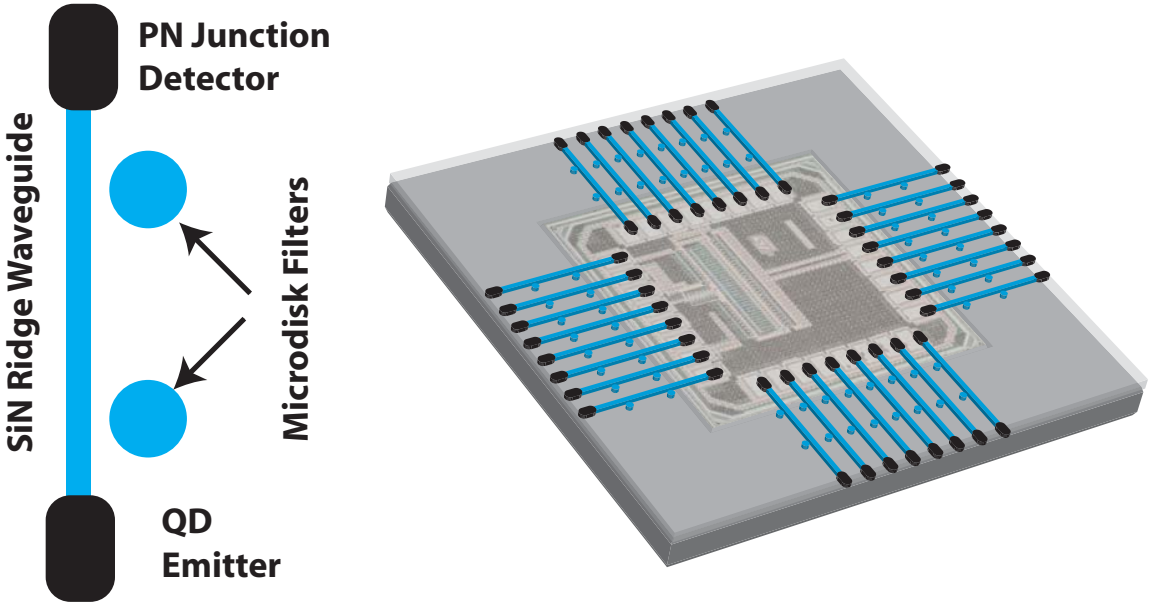

Figure 2: Illustration of a photonic guard ring to protect CMOS devices from HPM radiation. The circuit is only connected to the external world by SiN ridge waveguides. QD emitters are used as an internal source to communicate optically with a compact detector to create the optical data bus. In-line microdisk filters can be placed along the channel to reduce external noise and interference. These interconnects can be integrated monolithically onto the CMOS device as shown in the right picture. Once this is accomplished, the device is fully isolated from an electrical perspective from the external environment due to the enormous resistance of SiN.

trated in Fig. 2. We will develop optical interconnects composed of SiN ridge waveguides. SiN is fully insulating so these photonic channels will not permit any external HPM radiation to be guided. QD emitters can be locally deposited in conjugated polymer so that they can be electrically driven by the external circuit. A PN junction detector on the other side of the channel serves as a receiver to transduce the signal back to electrical. In addition, microdisk filters can be placed in-line to isolate a narrow spectral range and eliminate potential sources of noise from the environment. This ridge waveguides form a *photonic guard ring*, that can be used to protect critical components of a CMOS circuit. In particular, we are investigating an approach where a portion of a CMOS chip is guarded with photonic channels from the rest of the circuit, and stores copies of critical system parameters. Under HPM attack, the guarded circuit can quickly restore the system to a previous functioning state so that it can recover rather than experience a critical malfunction. A long-term goal would be to replace all inputs and outputs of a CMOS chip with photonic channels, as illustrated in the figure. This type of circuit would function just like a normal circuit, and could be incorporated into standard PC board systems, but would be fully HPM hardened against potential attack.

The PI is currently in a unique position to study photonic solutions for creating improved CMOS devices that are robust to HPM attack. The University of Maryland has one of the top research program in the area of HPM generation and device testing headed by Dr. John Rodgers. Both Dr. Waks and Dr. Rodgers are members of the Institute for Research in Electronics and Applied Physics (IREAP), which has one of the top programs in HPM research in the country. This project forms a natural point of connection between the two research groups. We will design CMOS devices with optical interconnects, and in collab-

oration with Dr. Rodgers we will use their expertise in HPM radiation to demonstrate improved performance of the photonic guard ring concept. This research could lead to significantly improved CMOS devices, and we anticipate a broad range of applications that would be of direct relevance to the mission of the AFOSR.

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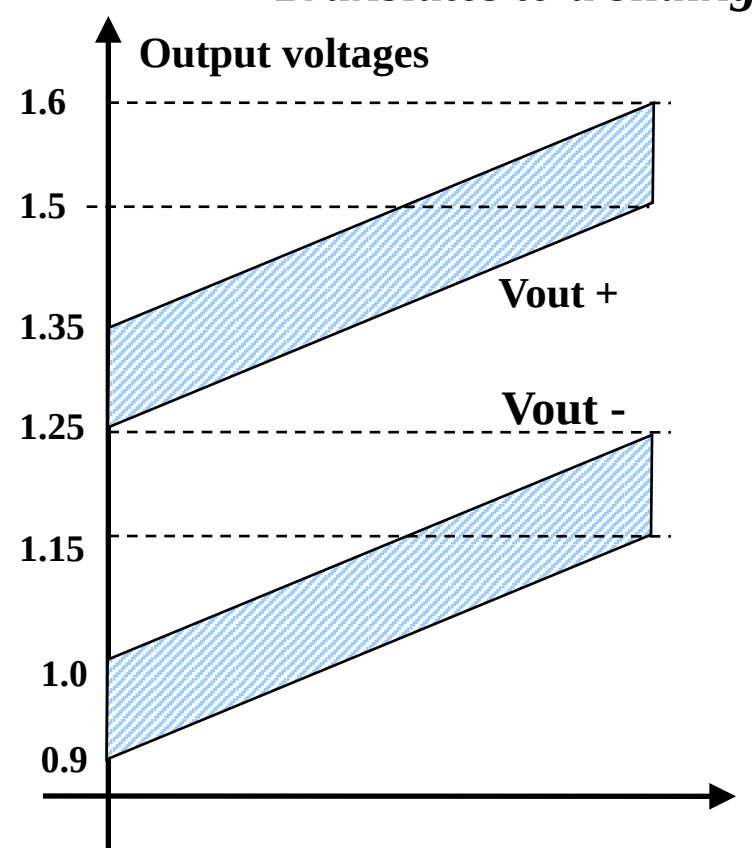
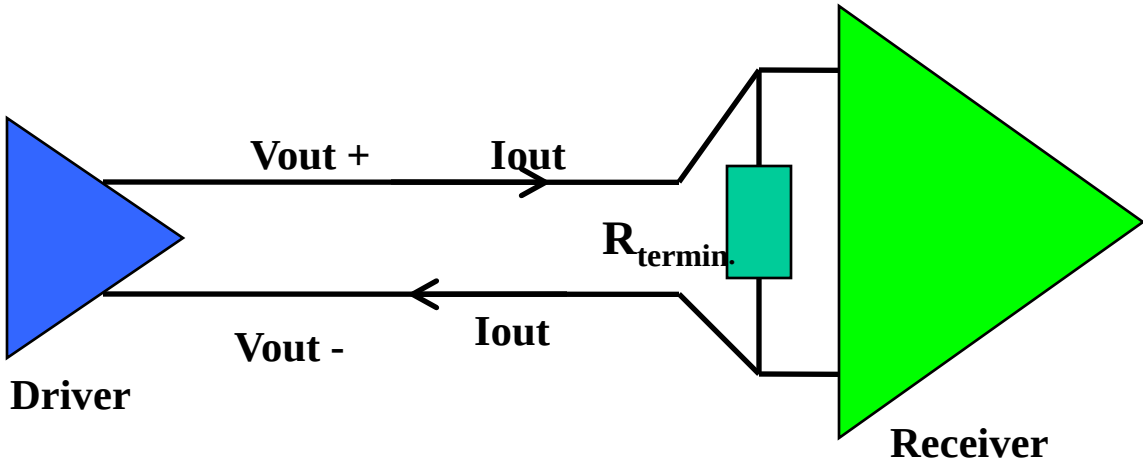
[5] V. L. Granatstein et al. Effects of High Power microwaves and Chaos in 21st Century Analog and Digital Electronics, 2001. MURI 2001 Final Report, October 31, 2006, http://www.ireap.umd.edu/MURI-2001/.

Introduction to LVDS

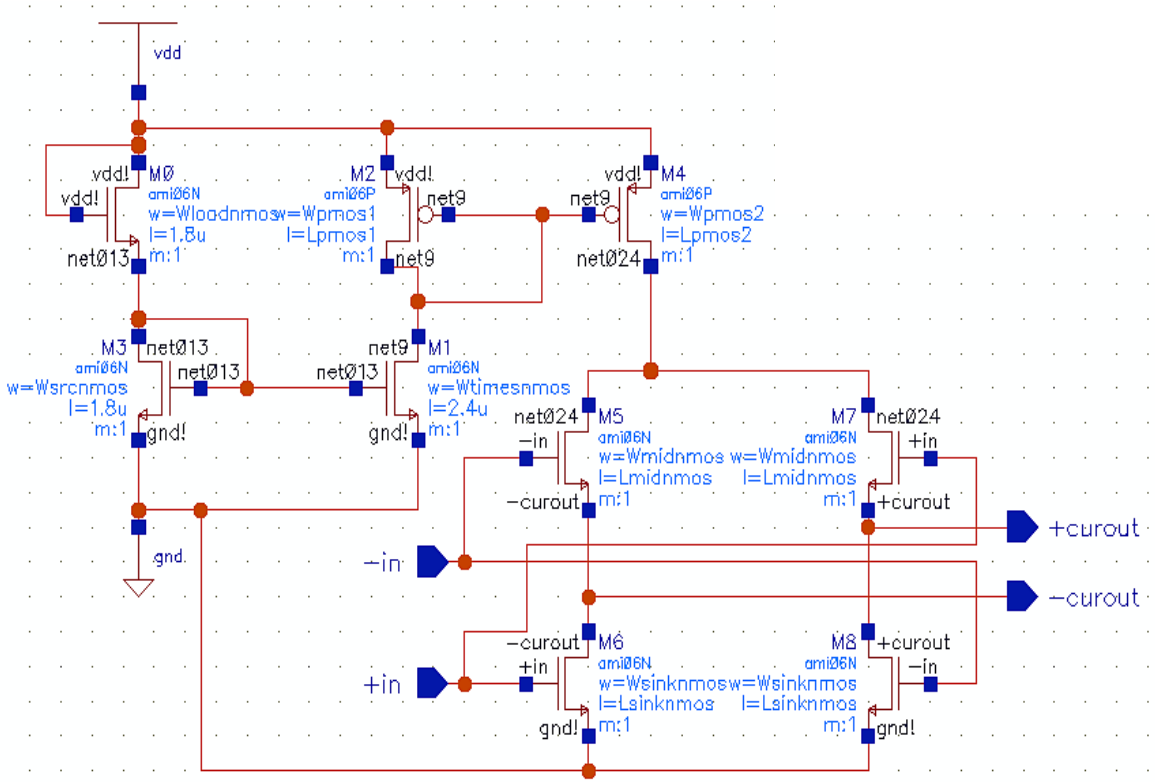
- **Low Voltage Differential Signaling**
- **ANSI/TIA/EIA-644-A (LVDS) standard**
  - **Differential output voltage V_{OD}: 247 to 454 mV**
  - **Offset voltage: 1.125 to 1.375 V**
  - ***Translates to a sliding range of voltages:***



  - **Termination resistor: 100 Ohm**
  - **Output current: V_{OD}/100; typically 3.5 mA**
  - **$t_{r/f}$=0.26 nsec min, 1.5 nsec max**

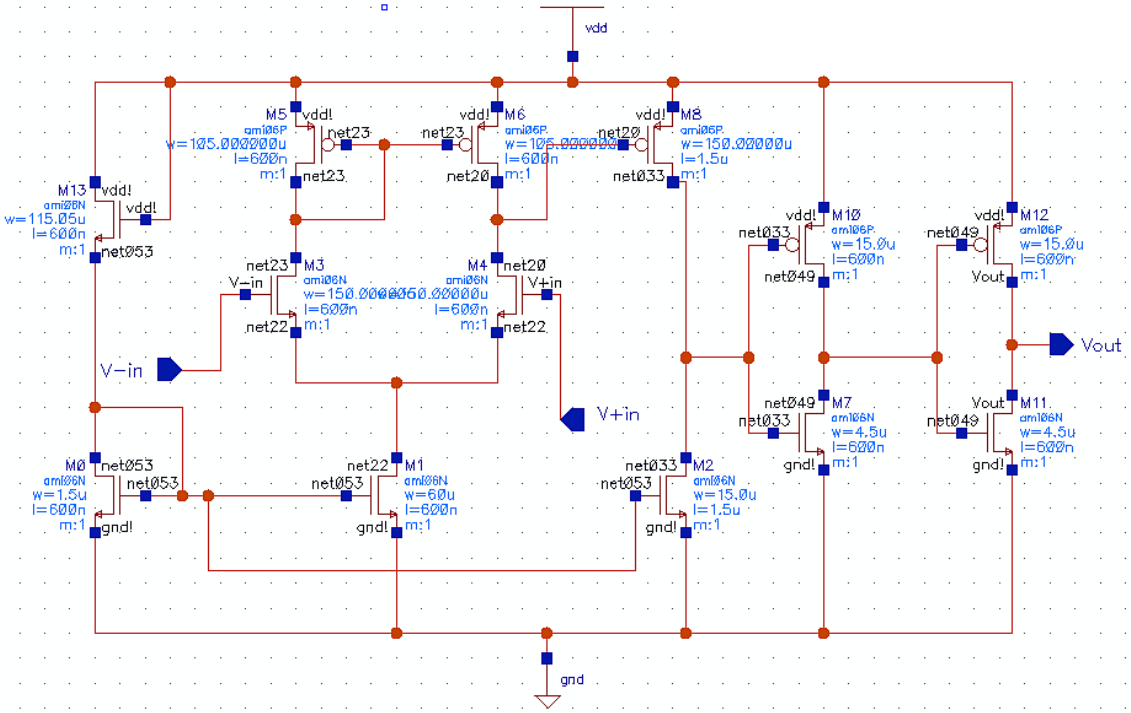


UMD-Designed LVDS Driver circuit



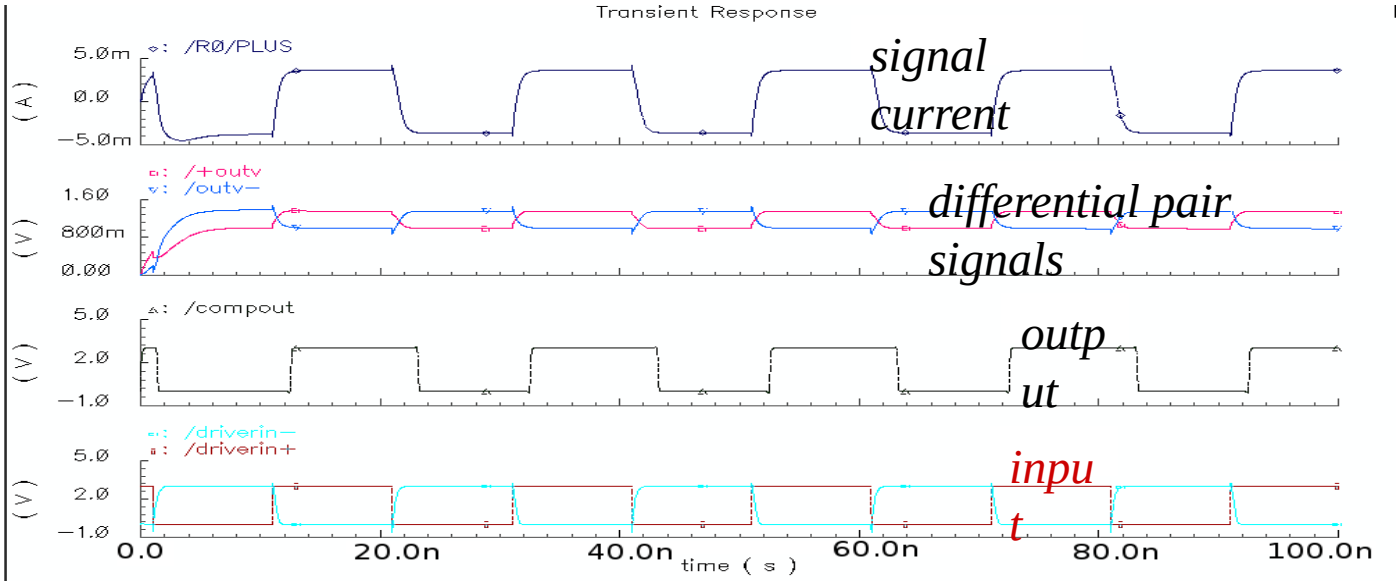
- Complementary voltage signals **+in** and **–in** as inputs
- Current either leaves **+curout** and enters back at **–curout** (output state HIGH) or leaves **–curout** and enters back at **+curout** (output state LOW)

Receiver circuit



- Simple comparator design
- Three stages: Differential amplifier, level shifter, digital buffer

Simulated LVDS Operation



Optimized operation:

I_{out} = 3.49 mA

V_{offset} = 1.155 V

t_f = 1.16 nsec

V_{od} = 350 mV

t_r = 0.94 nsec

Trace load: 8 pF

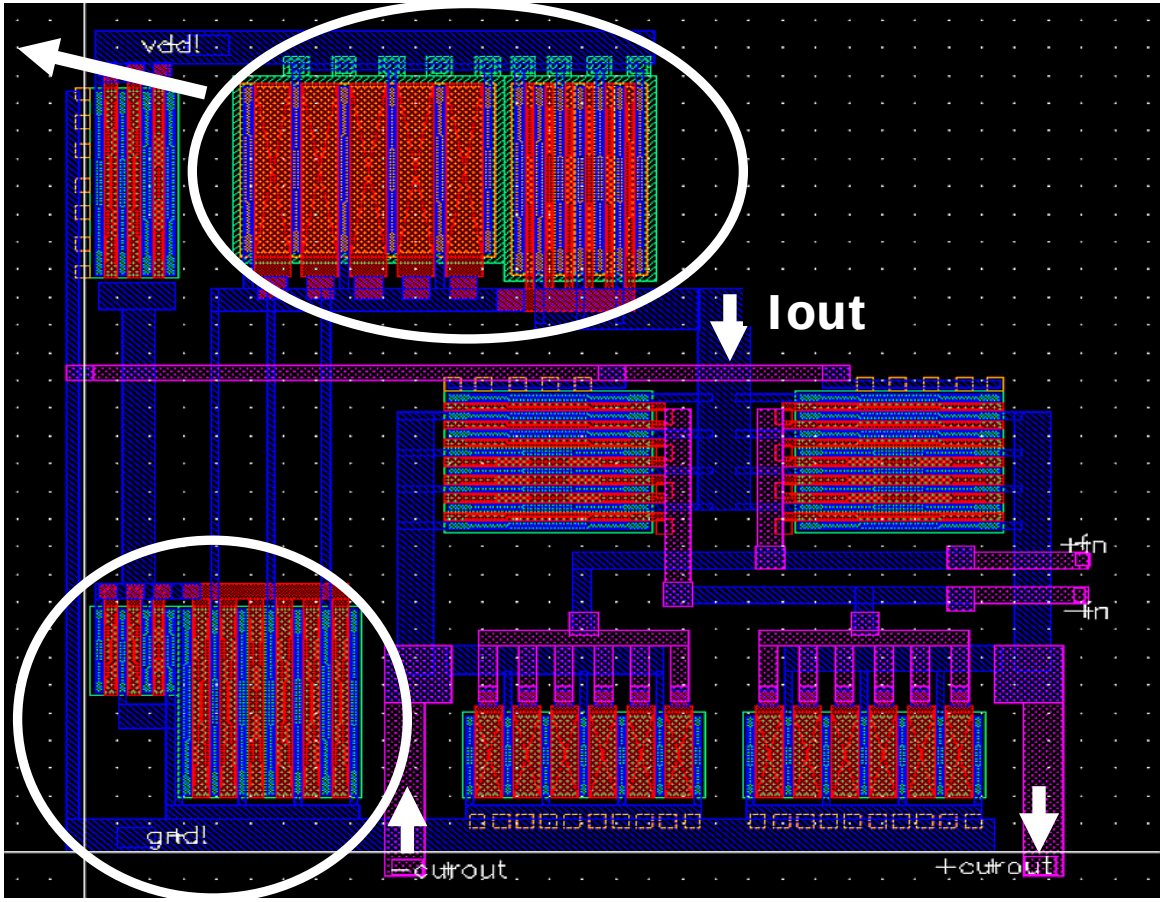
Red Line, Lowest Strip: INPUT

Black Line, Second-Lowest Strip: OUTPUT

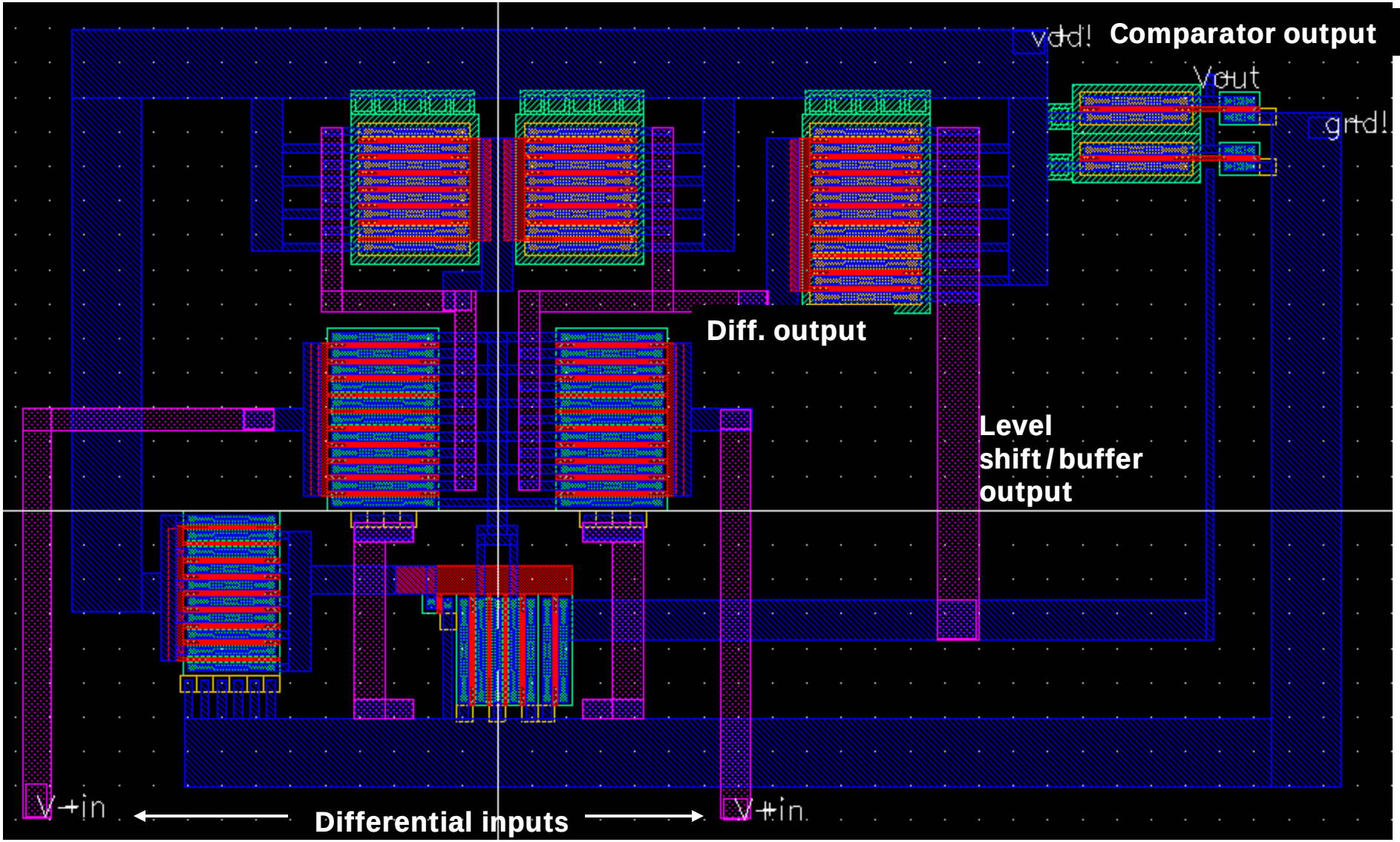
VLSI layout of LVDS Circuit

PMOS current mirror

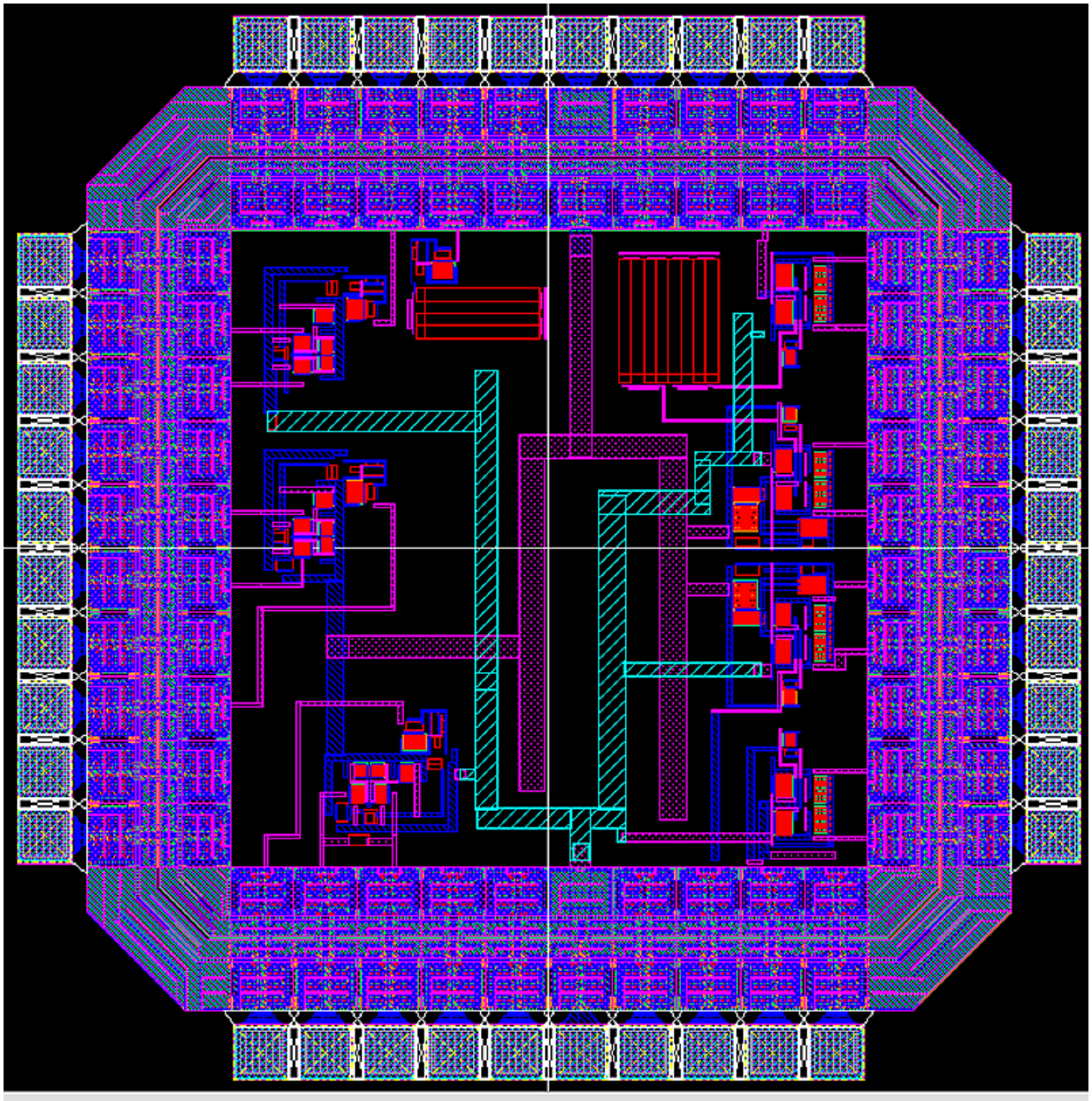
NMOS current mirror



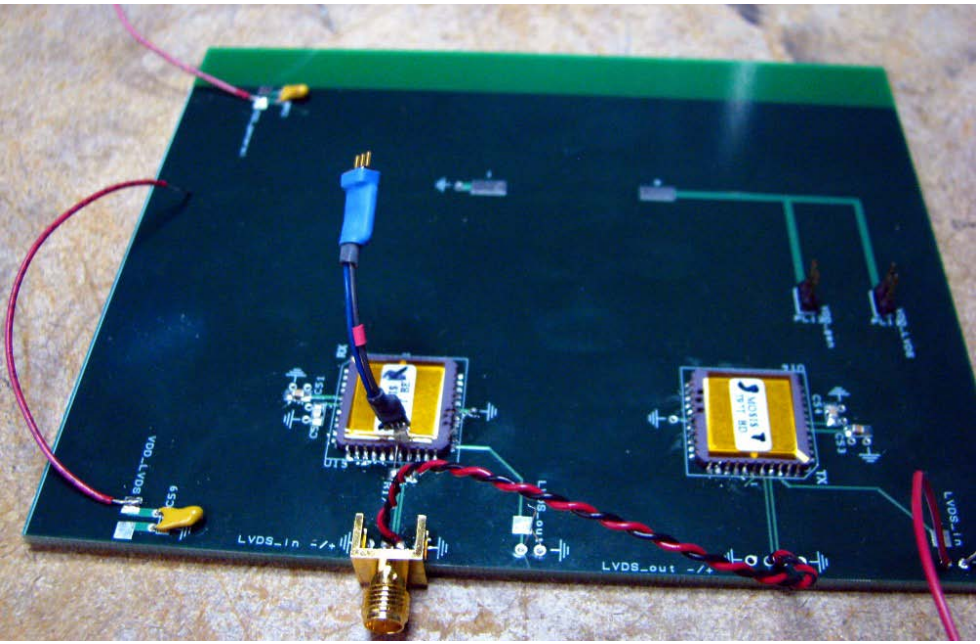
Receiver VLSI Layout



Transmitter Full Chip Layout



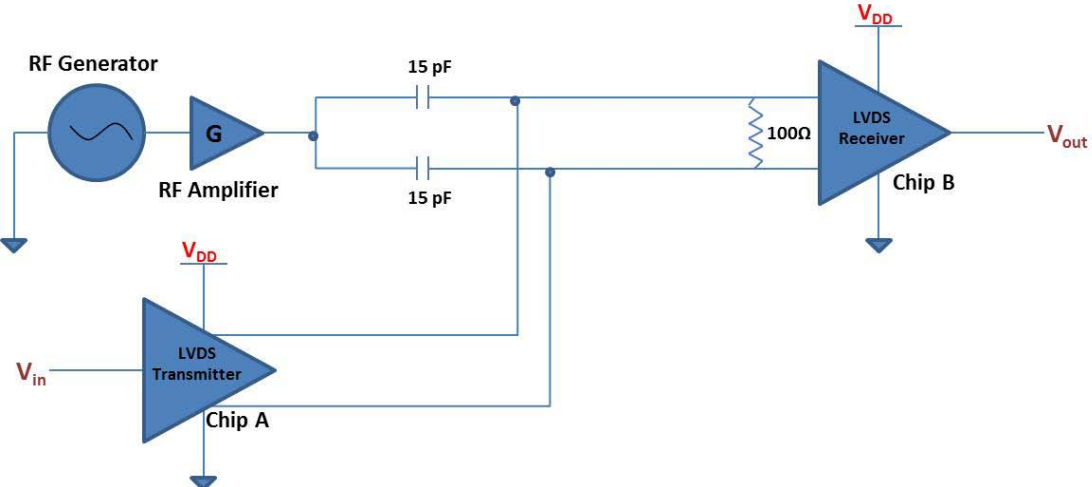
TEST SETUPS

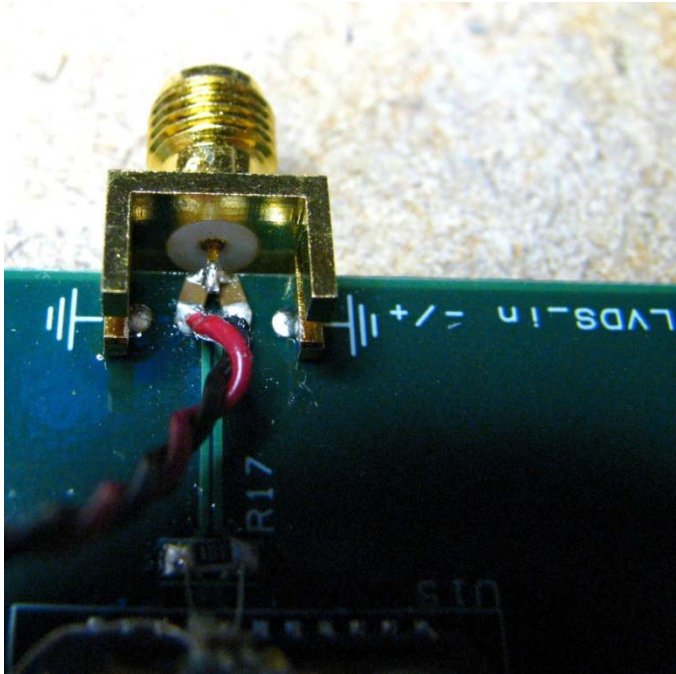


Left: Full LVDS system test board

Bottom: Injection point detail

Bottom left: Test system schematic





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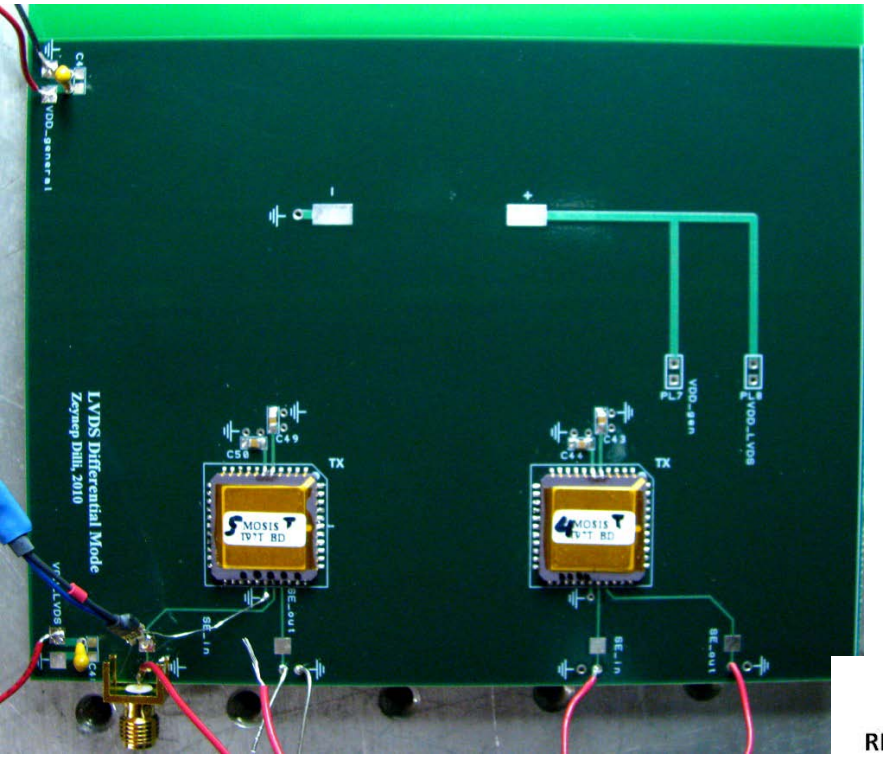
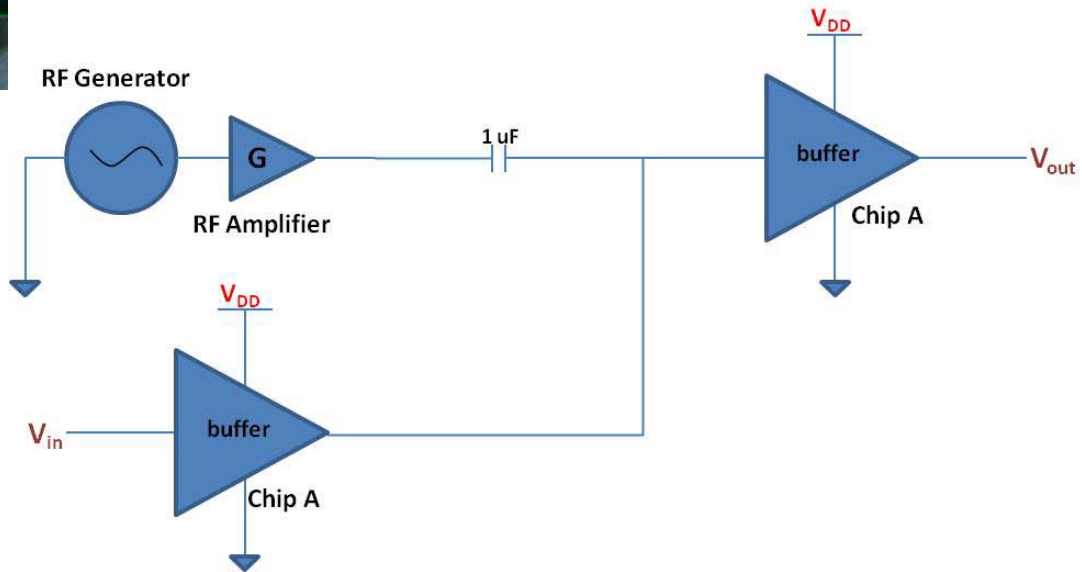


Left: SE system test board

Bottom: Test system schematic



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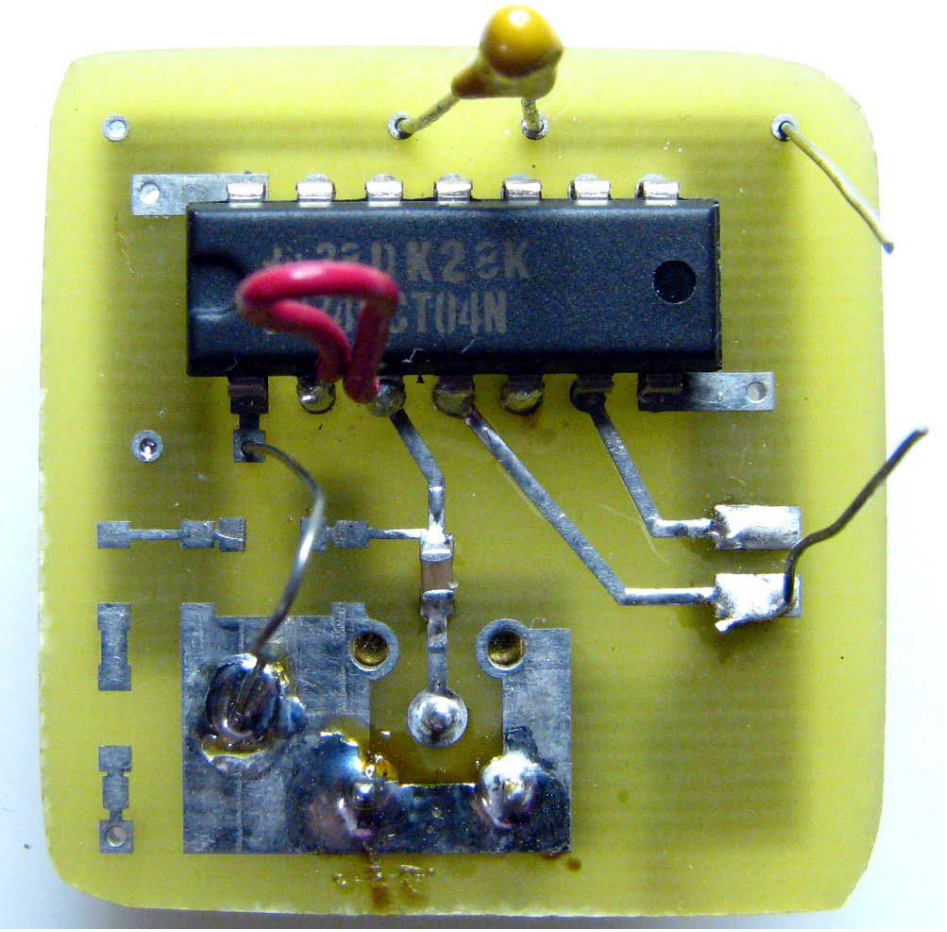
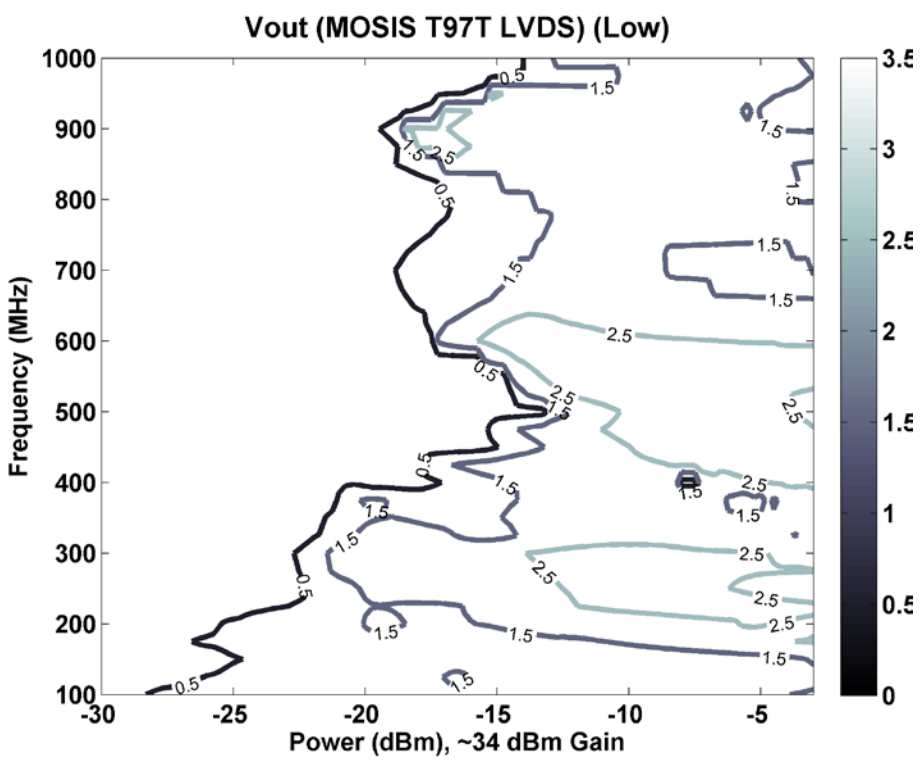


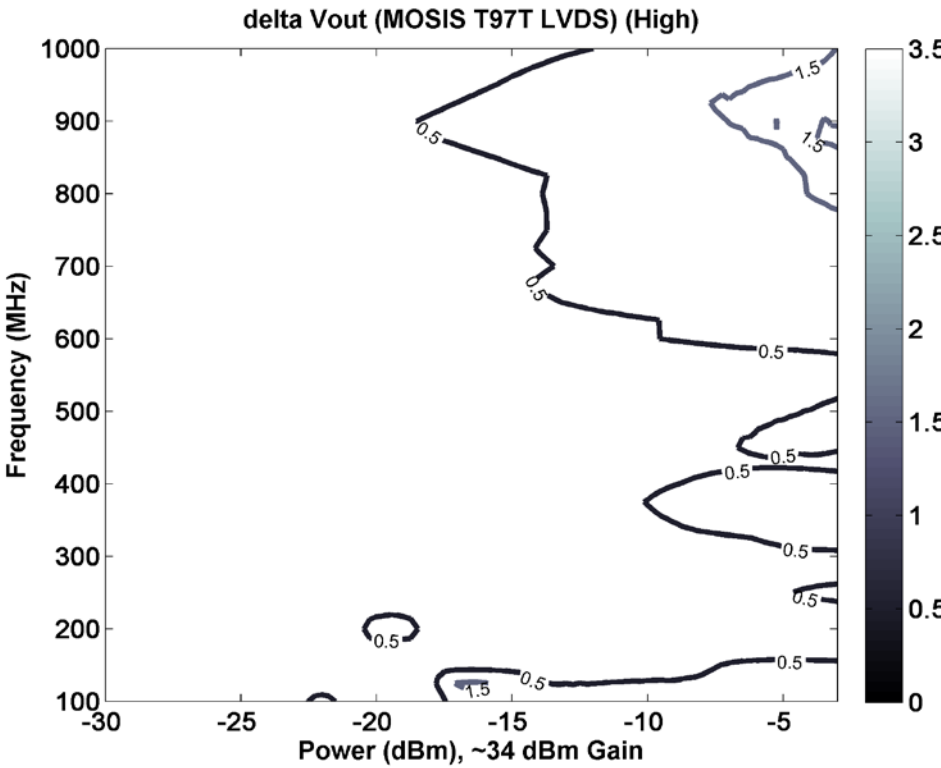
Left: A commercial system test board

Tested:

- LVDS: National Semiconductor DS90
- LVDS: Texas Instruments SN65
- SE: Fairchild HCT04SE
- SE: TI …?

TEST RESULTS



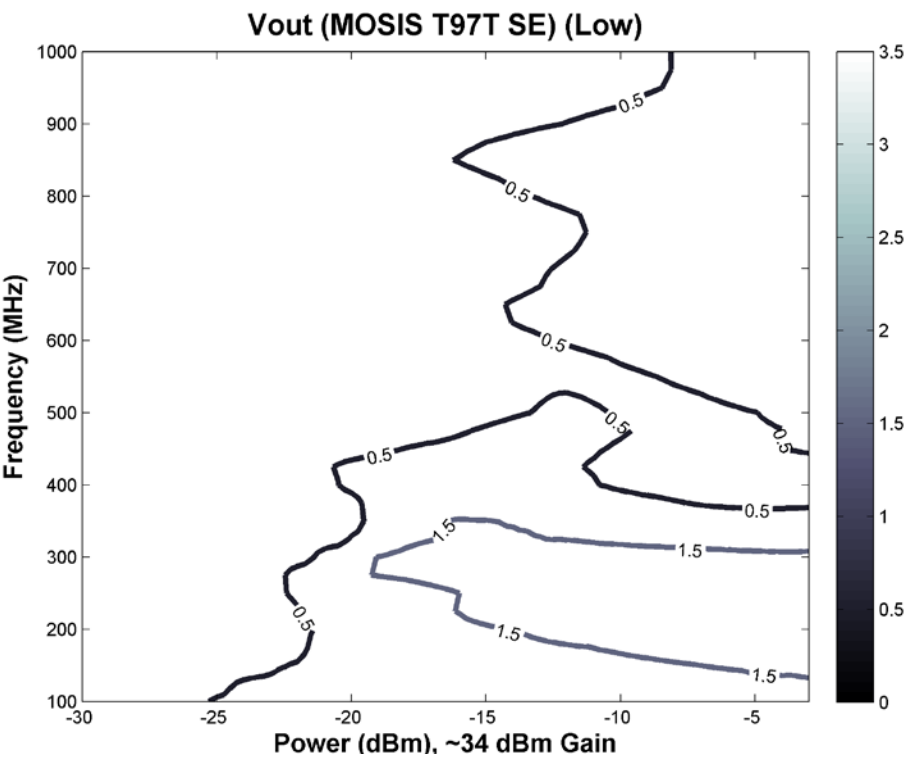


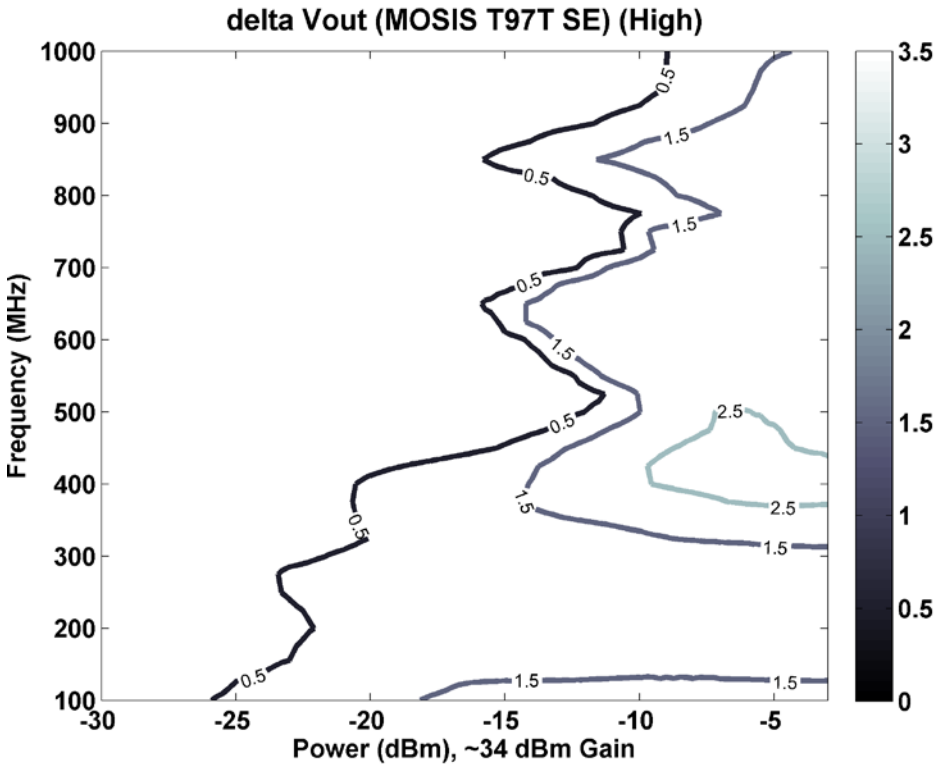
LVDS first generation test results

Left: Output (V_{out}) for input low

Right: Delta-V output (V_{dd}-V_{out}) for input high ***(Almost no errors)***

TEST RESULTS





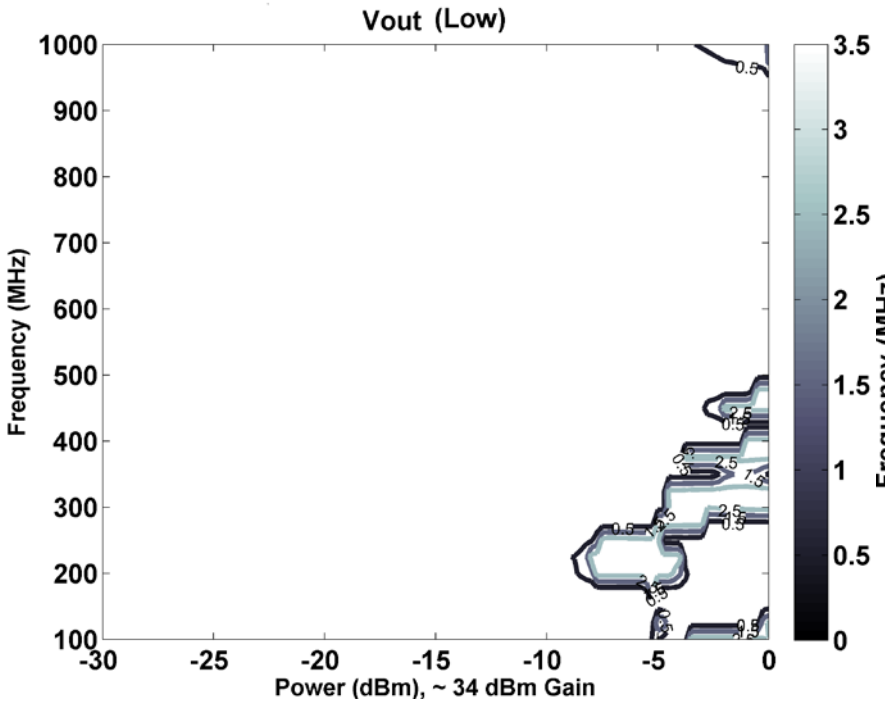
SE test results

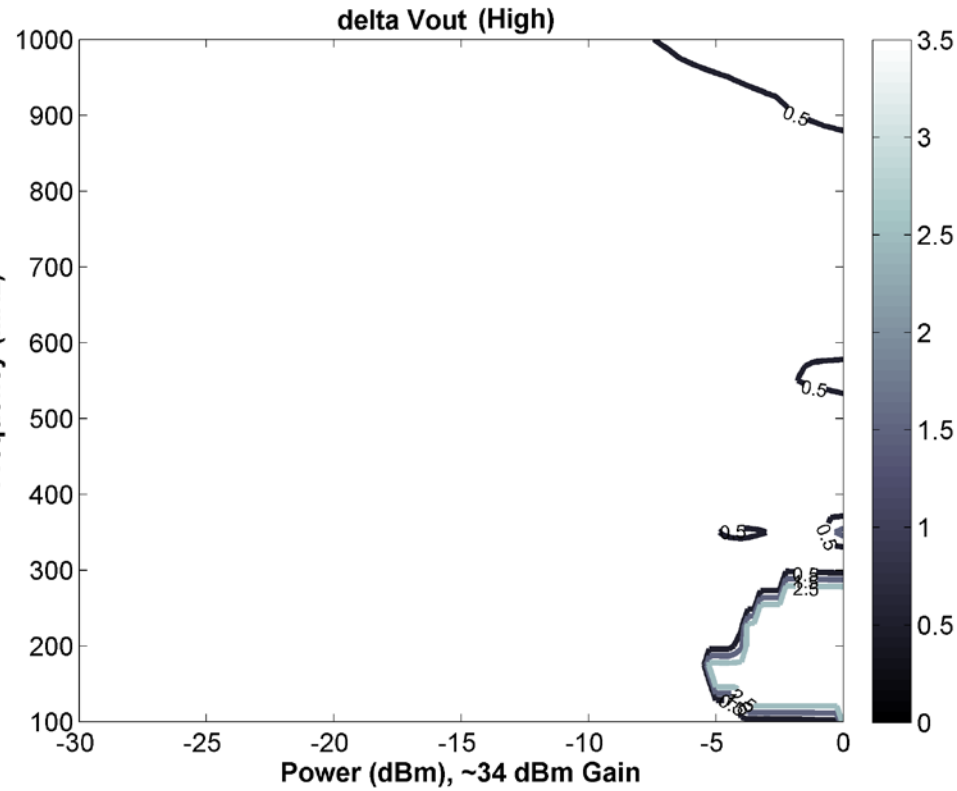
Left: Output (V_{out}) for input low

Right: Delta-V output (V_{dd}-V_{out}) for input high

Comparison: Low state; SE is less vulnerable (over low frequencies only, though not much power difference). High state: LVDS is much less vulnerable.

TEST RESULTS



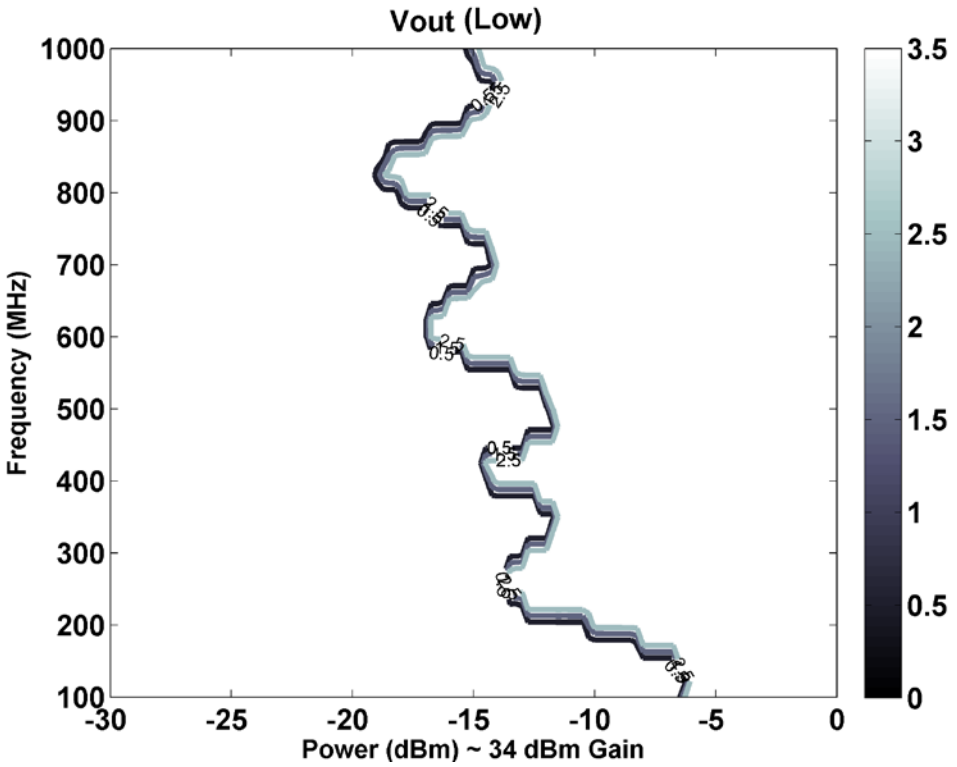


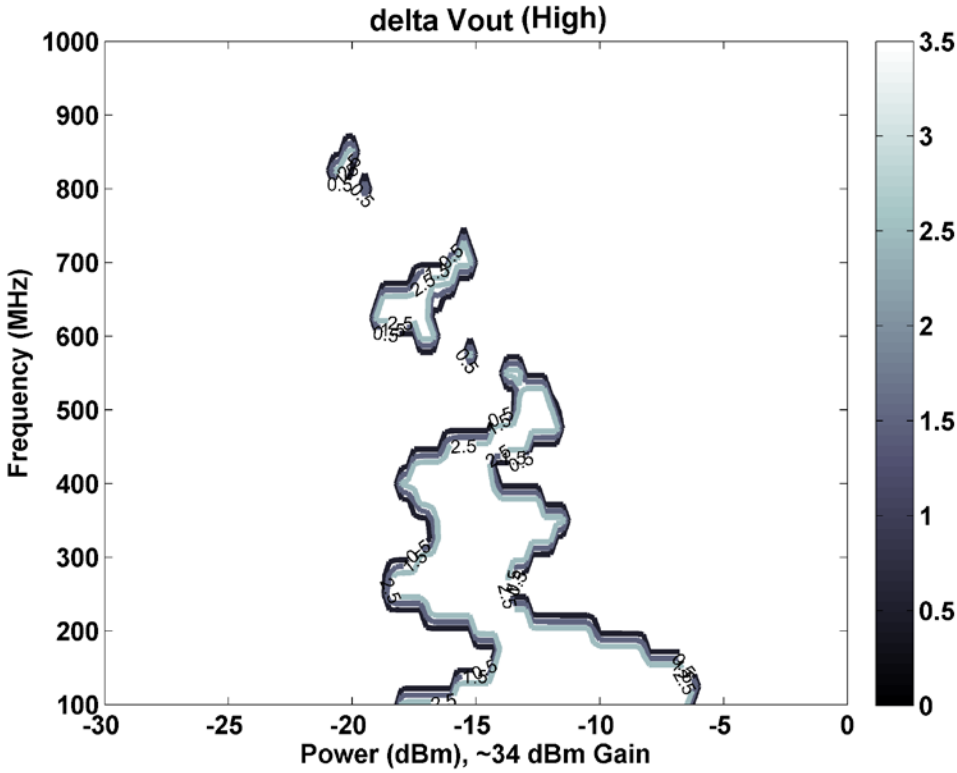
Commercial LVDS1 test results

Left: Output (V_{out}) for input low

Right: Delta-V output (V_{dd}-V_{out}) for input high

TEST RESULTS



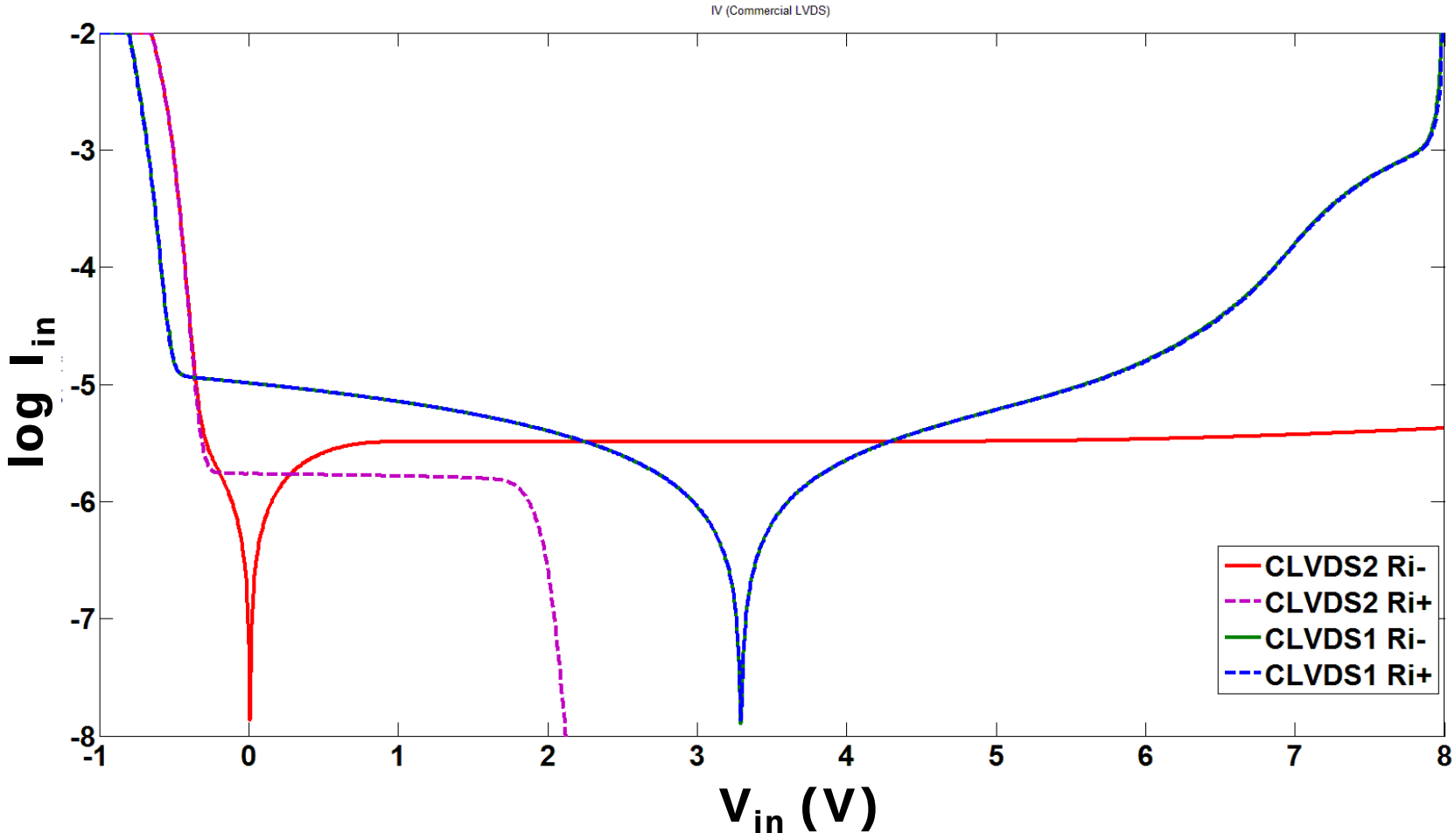


Commercial LVDS2 test results

Left: Output (V_{out}) for input low; Right: Delta-V output (V_{dd}-V_{out}) for input high

Comparison: LVDS1 is much more robust both in high and in low states. It very likely has a different ESD structure. Both commercial chips have higher gain than our first generation.

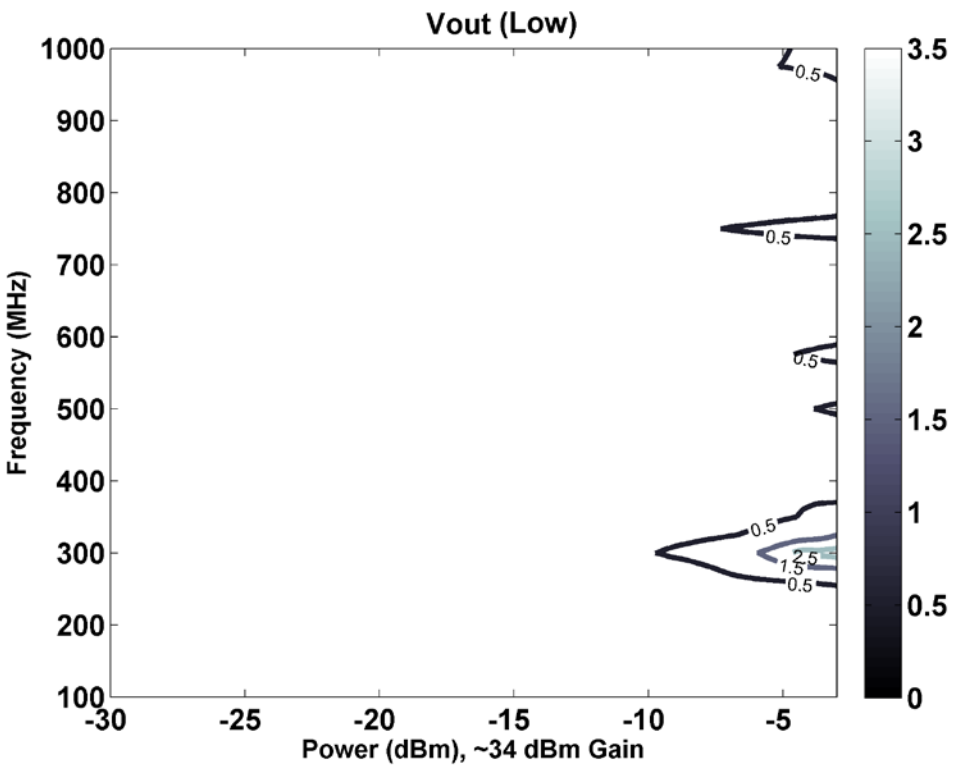
TEST RESULTS

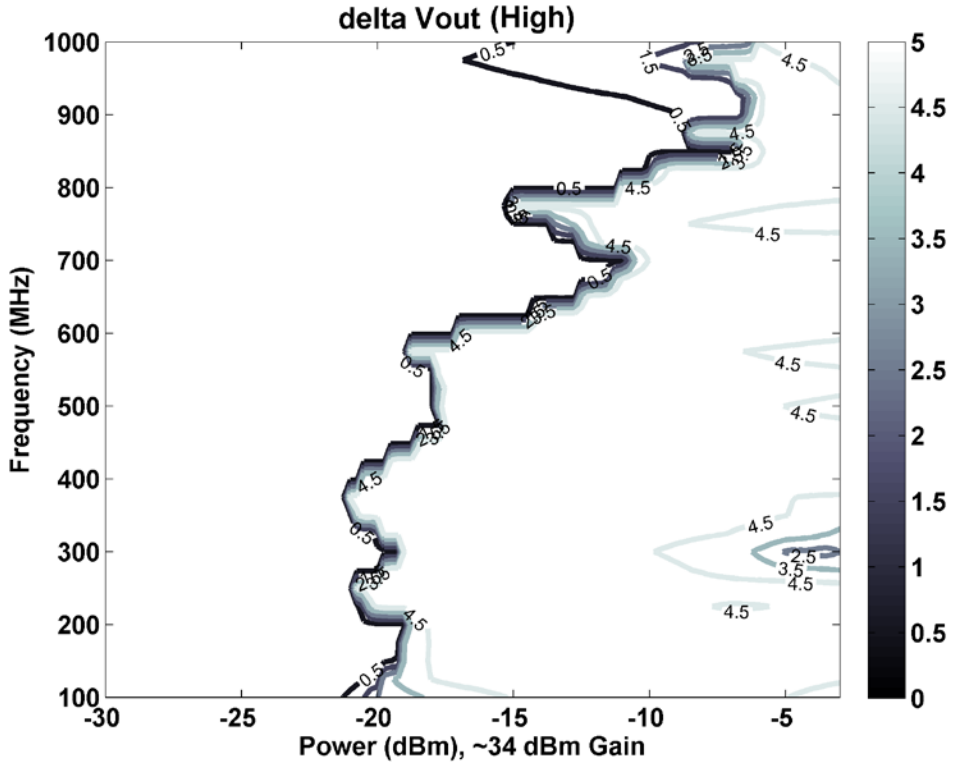


The IV curves measured at the input pins of the commercial LVDS1 and LVDS2 integrated circuits indicate different ESD architectures.

This is partly responsible for the difference in HPM vulnerability.

TEST RESULTS





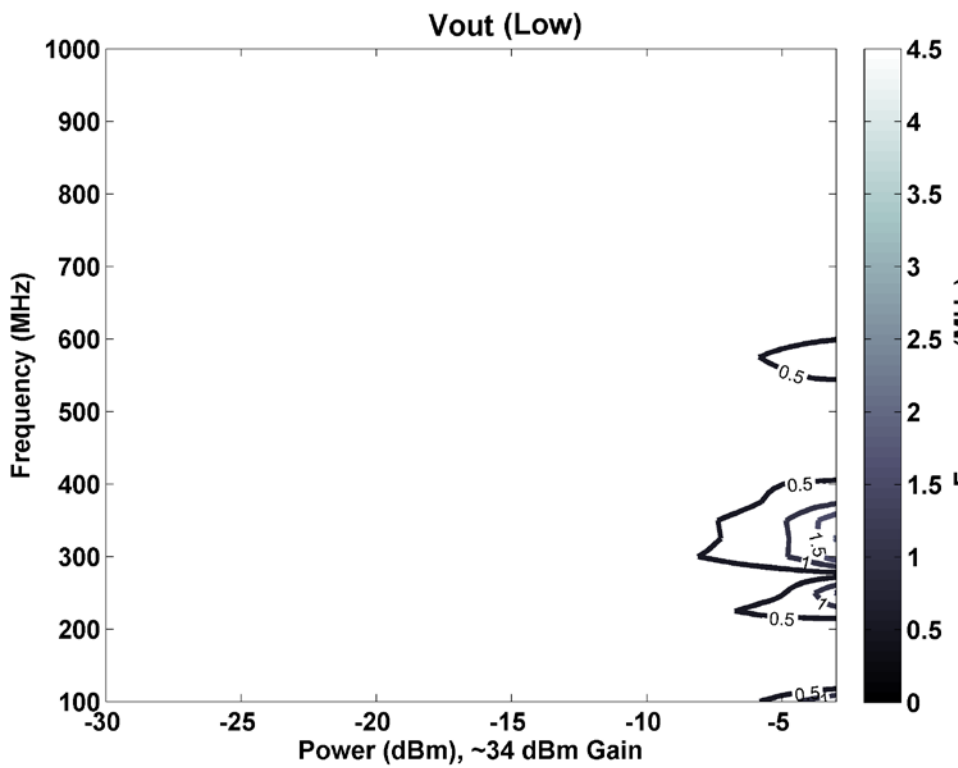
Commercial SE1 test results

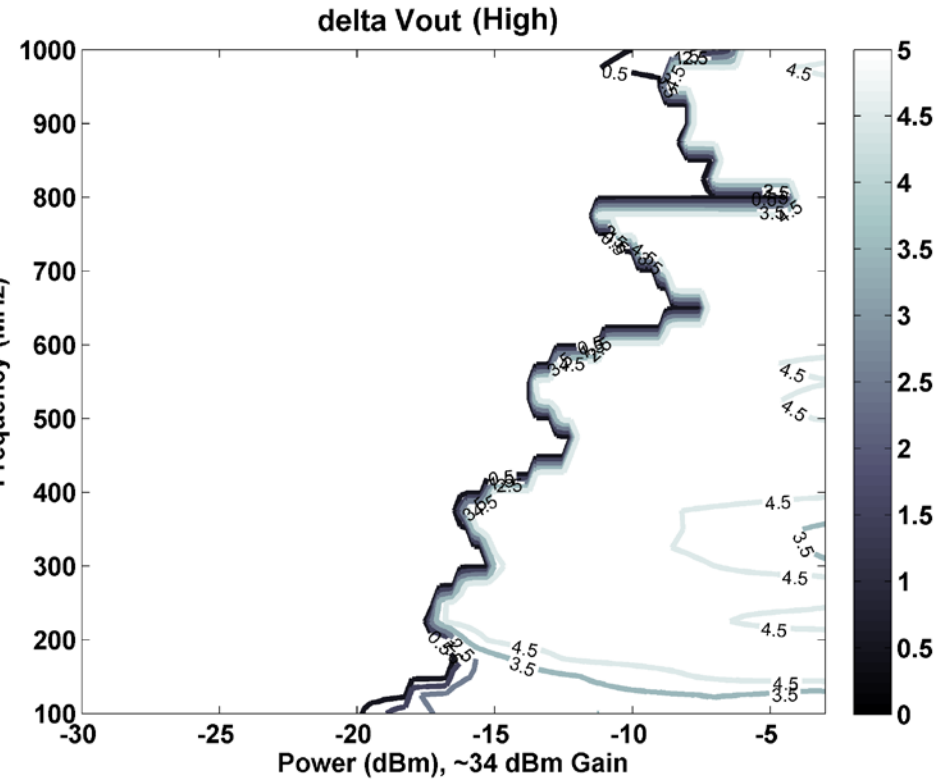
Left: Output (V_{out}) for input low

Right: Delta-V output (V_{dd}-V_{out}) for input high ***(NOTE: THIS DEVICE HAS Vdd=5 V instead of 3)***

Comparison: High is very vulnerable; low has almost no errors

TEST RESULTS





Commercial SE2 test results

Left: Output (V_{out}) for input low

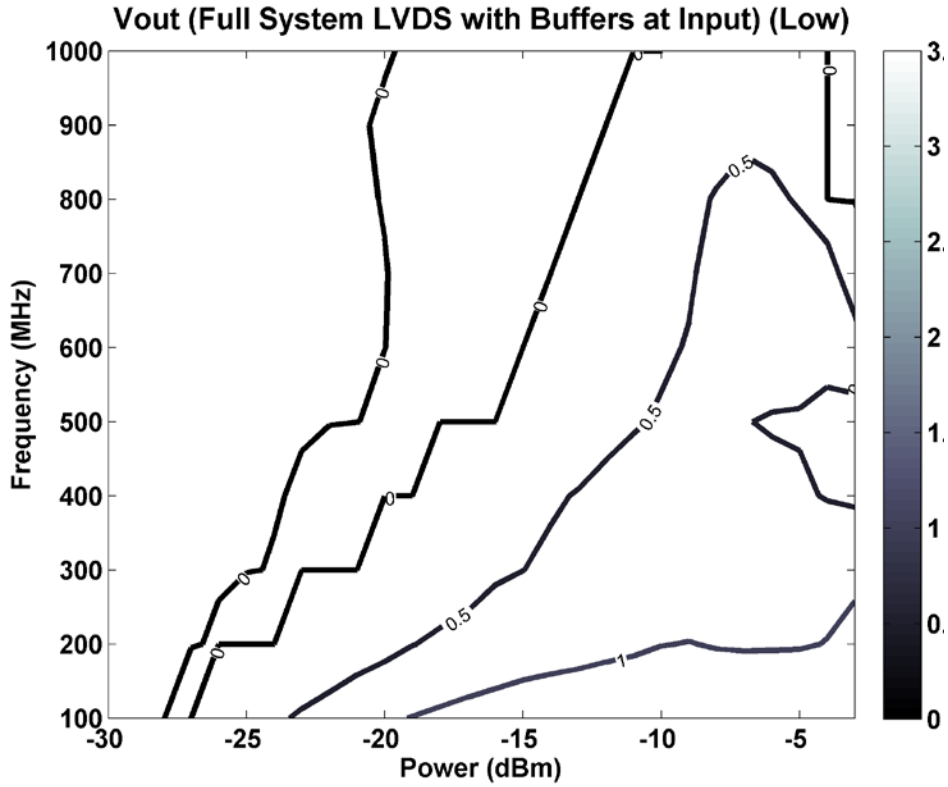
Right: Delta-V output (V_{dd}-V_{out}) for input high ***(NOTE: THIS DEVICE HAS Vdd=5 V instead of 3)***

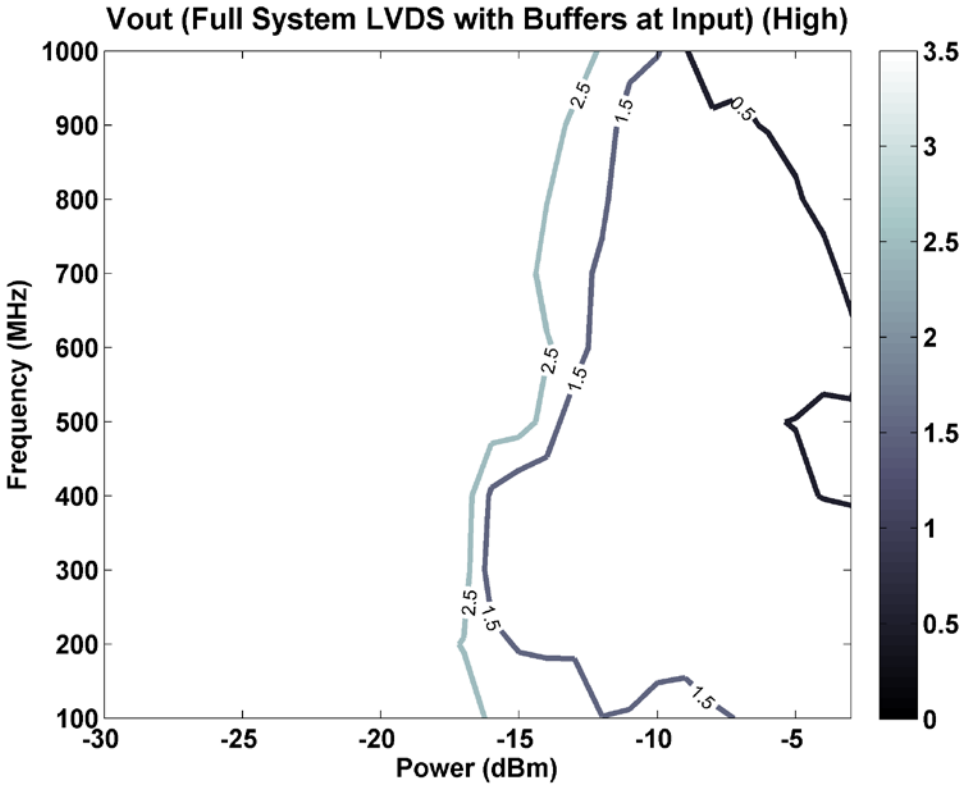
Comparison: High is very vulnerable; low has almost no errors. Both commercial SE devices behave similarly. For high, LVDS1 is much less vulnerable; LVDS2 is somewhat less vulnerable (a certain power range for low frequencies).

SECTION: SIMULATION RESULTS

- We have modified designs for both transmitter and receiver
  - Transmitter: Trade-off between voltage levels and vulnerability
  - Receiver: Higher gain

SIMULATION RESULTS





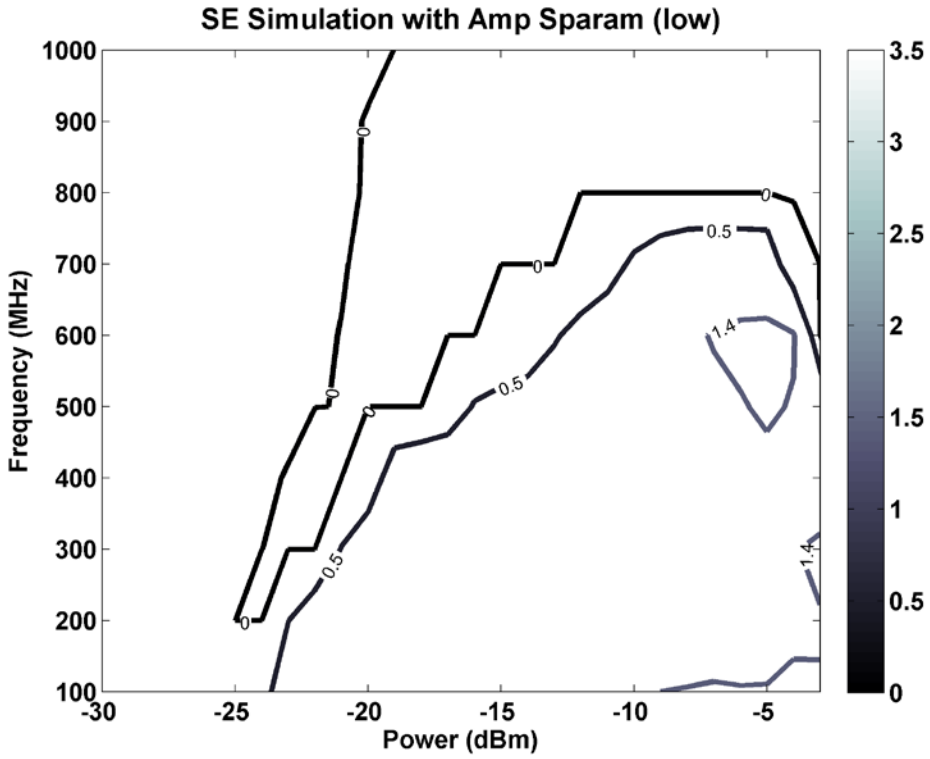
LVDS first generation simulation results

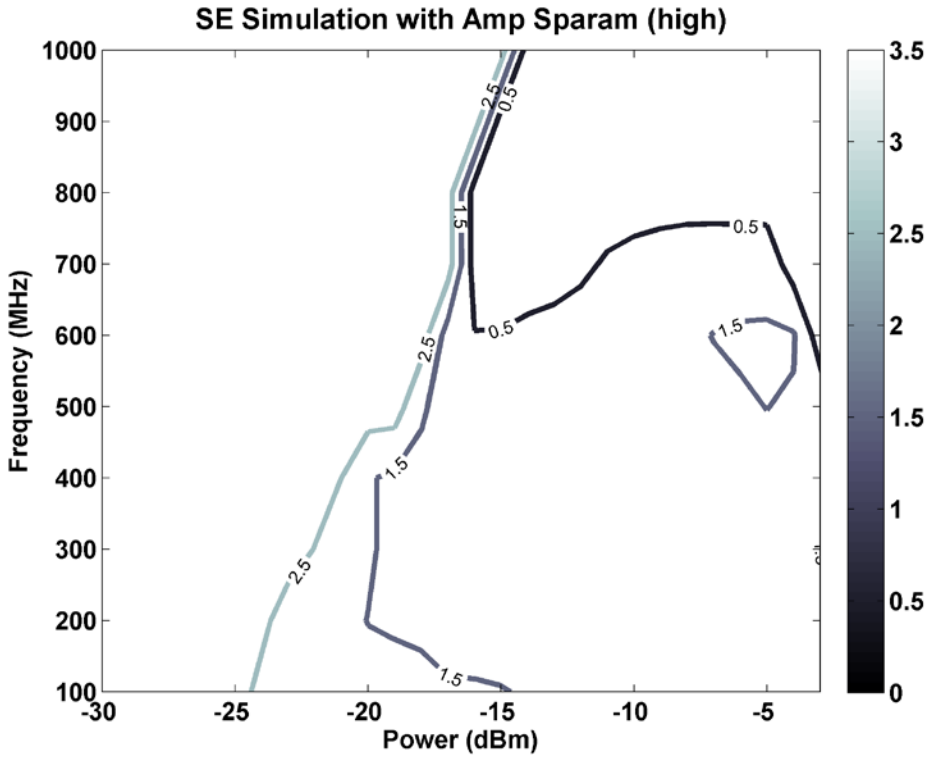
Left: Output (V_{out}) for input low

Right: Output (V_{out}) for input high

Comparison: Low has no errors; high is uniformly vulnerable after a certain power. This is the exact opposite of what's measured…

SIMULATION RESULTS





SE simulation results

Left: Output (V_{out}) for input low

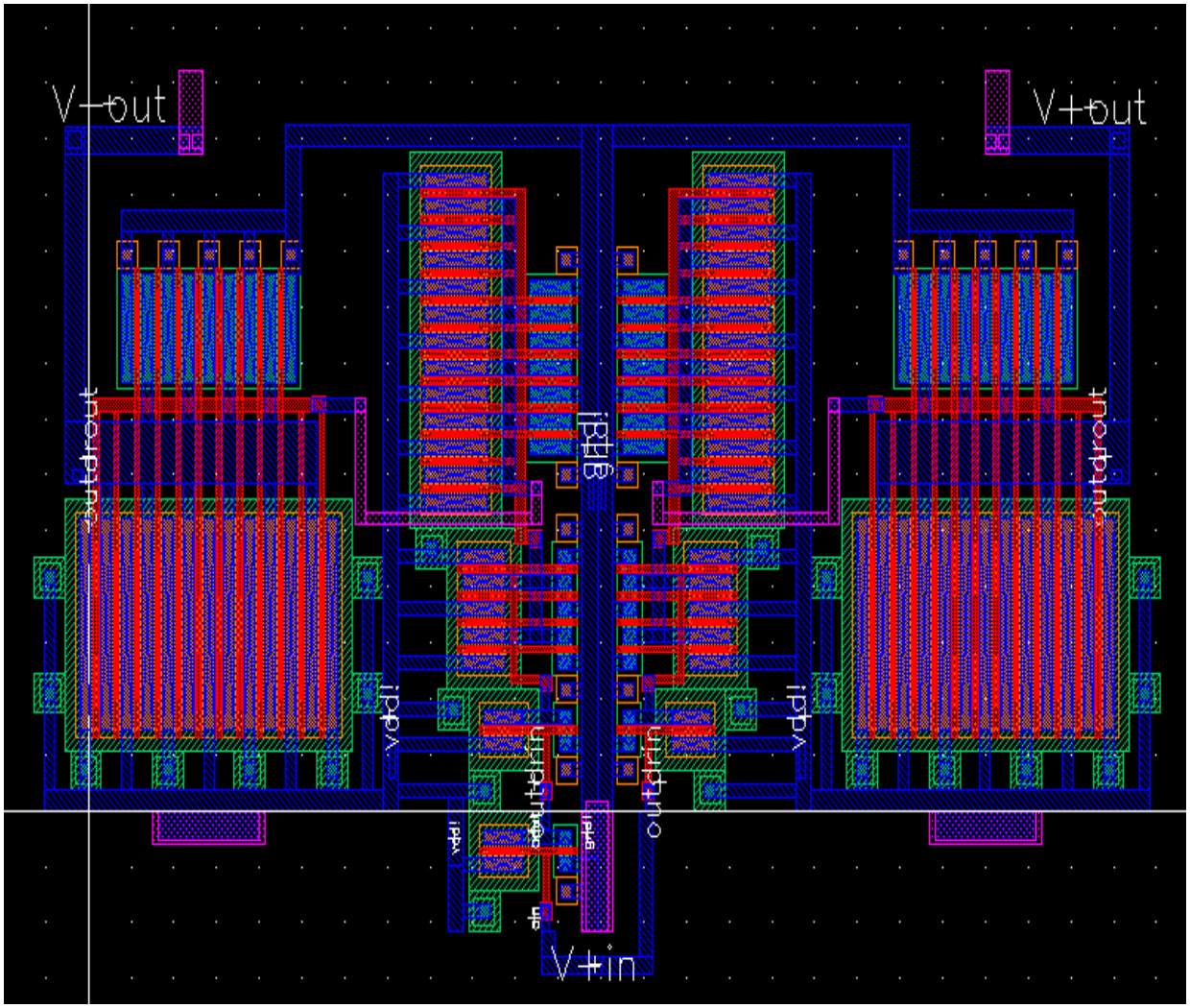
Right: Output (V_{out}) for input high

Comparison: Low has almost no errors; high is uniformly vulnerable after a certain power. For the high state LVDS is slightly less vulnerable; it takes 3 to 5 dBm higher input power for a erroneous switch. In the measurement results that difference is more pronounced.

SECTION: MITIGATION

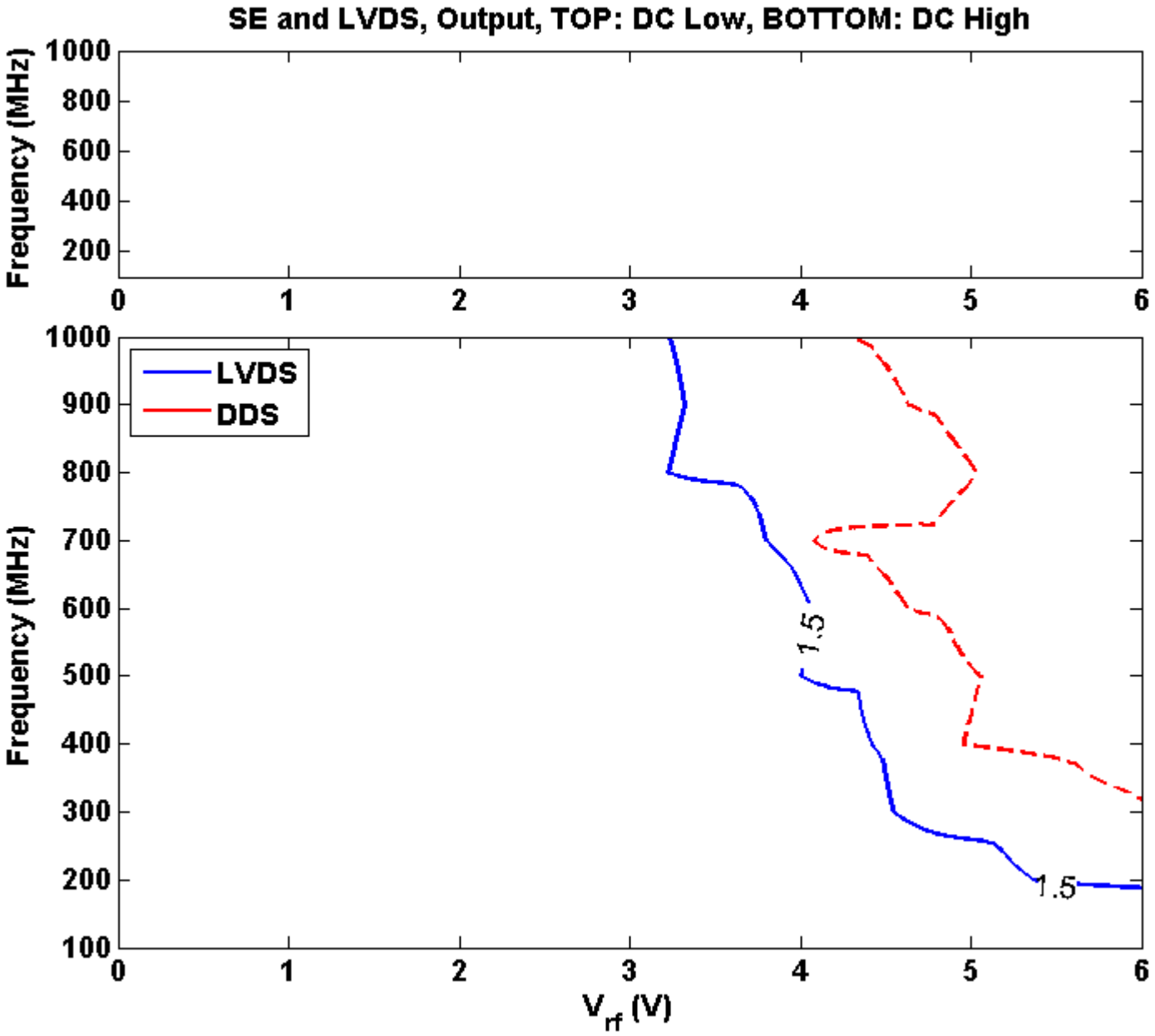
- We have modified designs for both transmitter and receiver structures
  - Mitigation in the transmitter: Trade-off voltage levels and power consumption for vulnerability
  - Mitigation in the receiver: Design with a common-mode-rejection ratio
- These circuits have been fabricated and are now under test

Mitigation I: Trading off Low Voltage



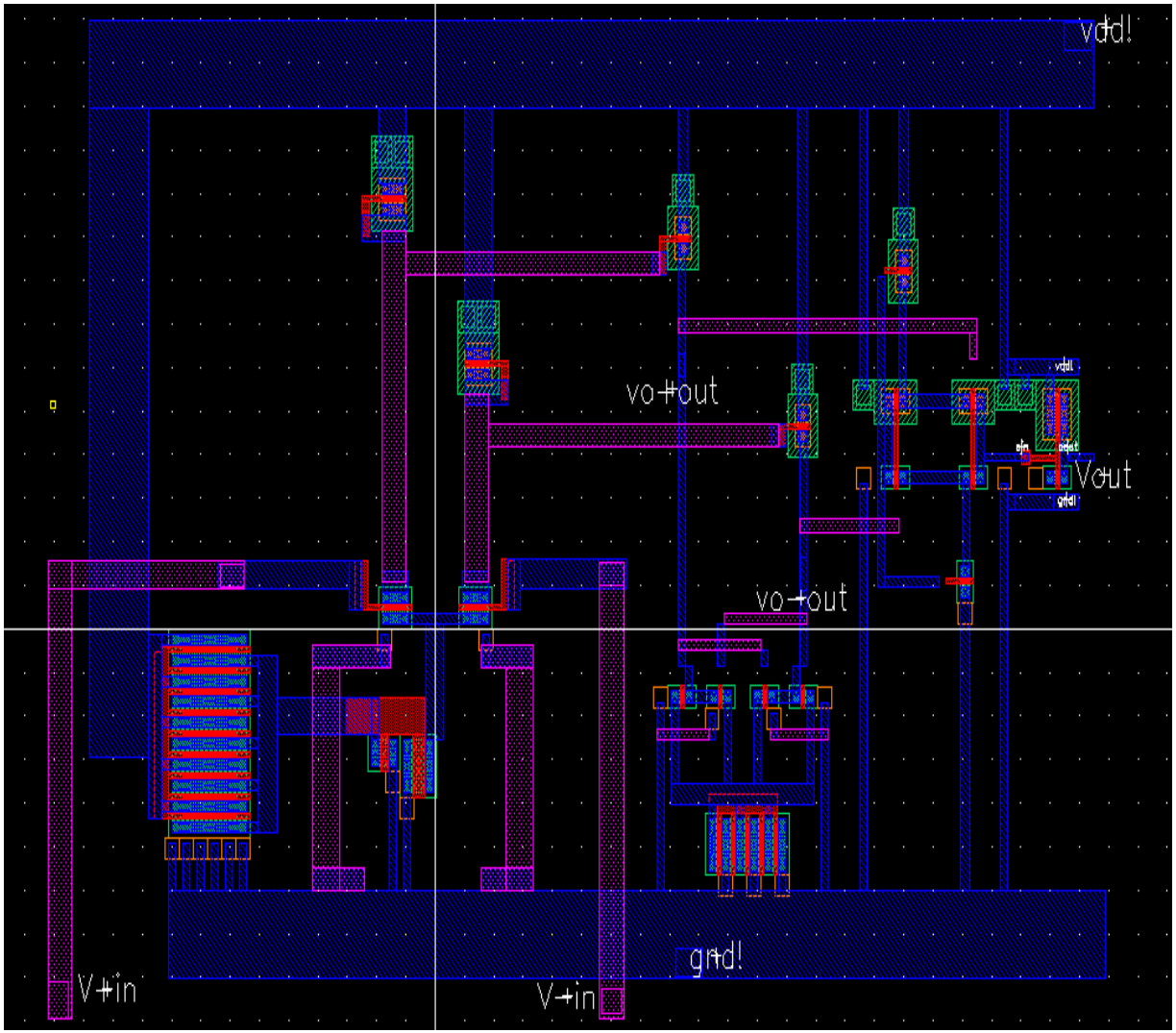
Digital DS (“DDS”) Driver: Differential pair output with full ground-to-rail swing

Mitigation I: Trading off Low Voltage for Immunity



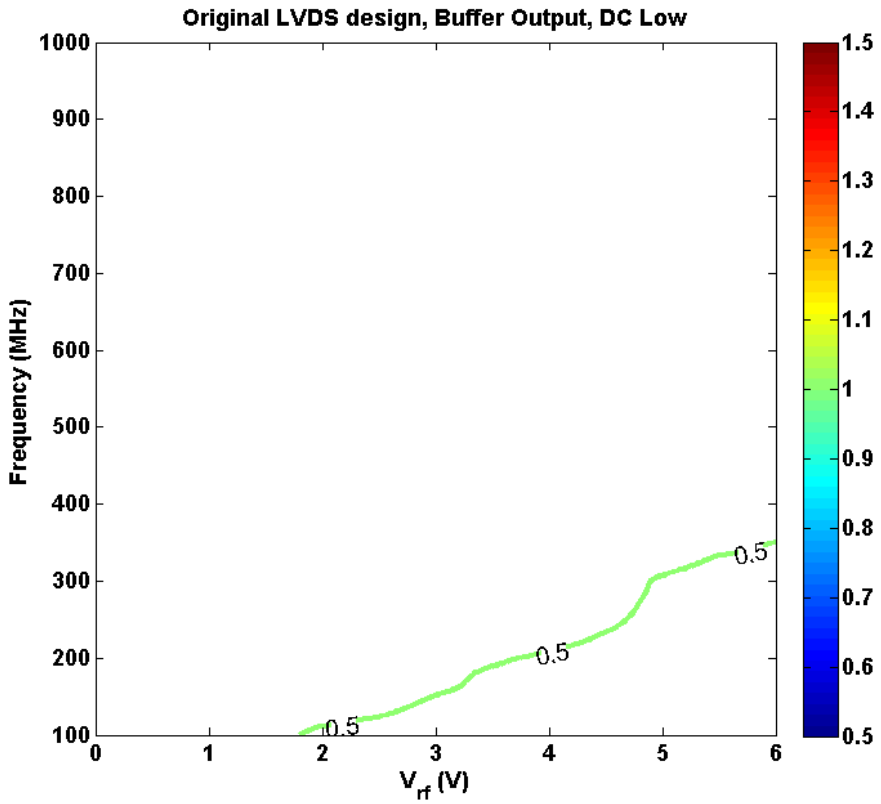
Digital DS ("DDS") Driver: Vulnerability limit at higher HPM power in the high-state (Blue: original LVDS; Red: DDS)

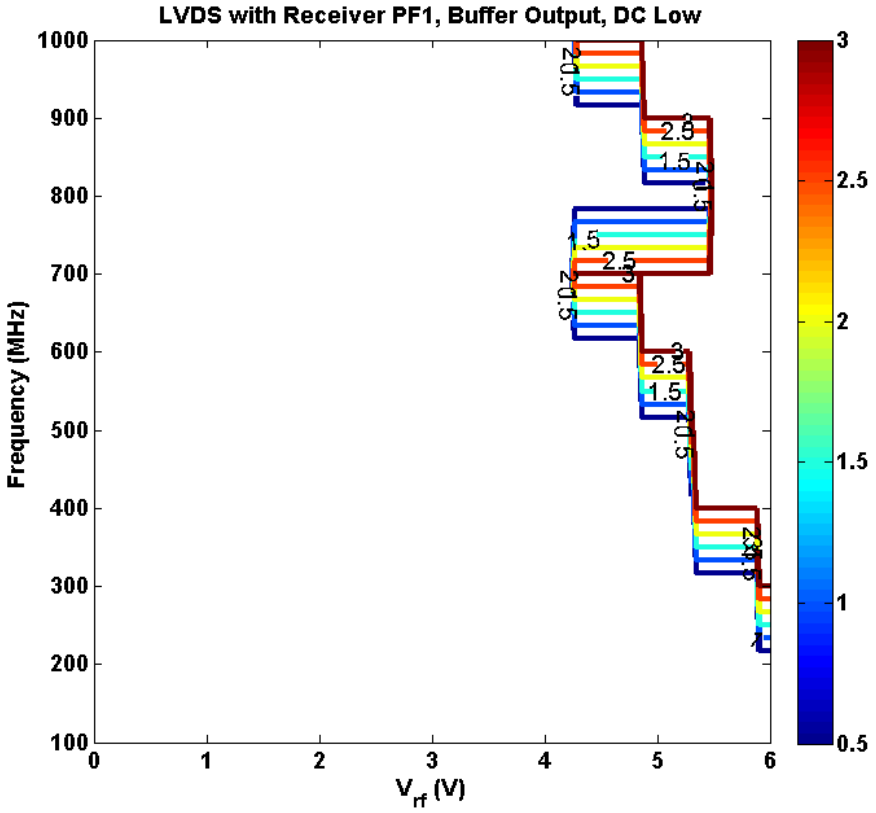
Mitigation II: Rethinking the Receiver



Updated comparator design with internal positive feedback as the differential signal receiver: Higher common-mode rejection

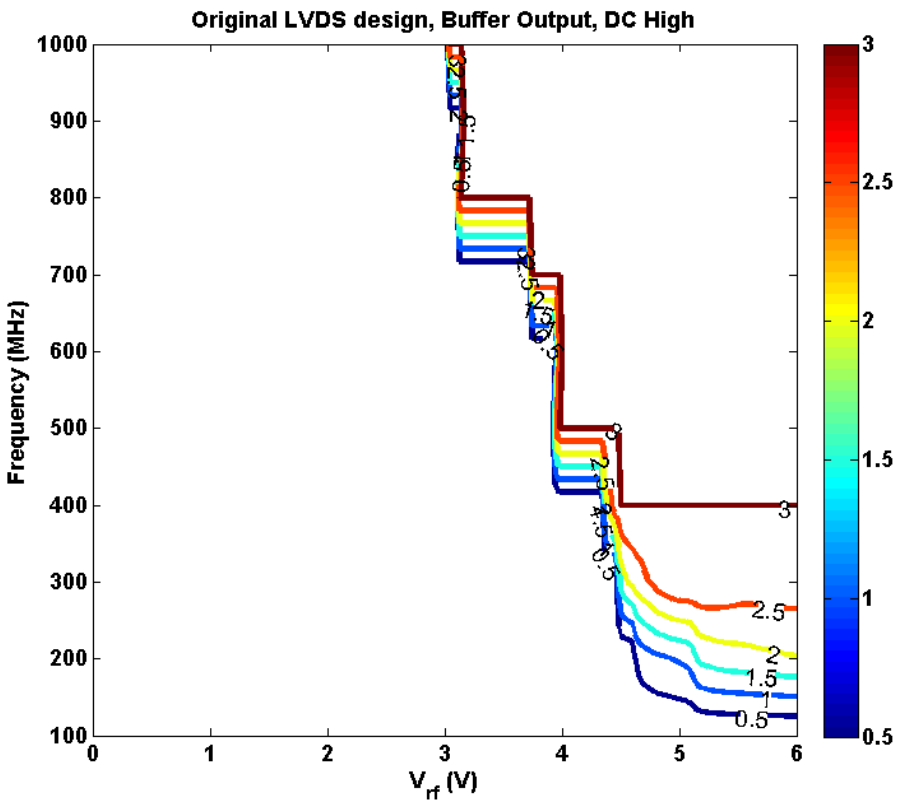
Mitigation II: Rethinking the Receiver

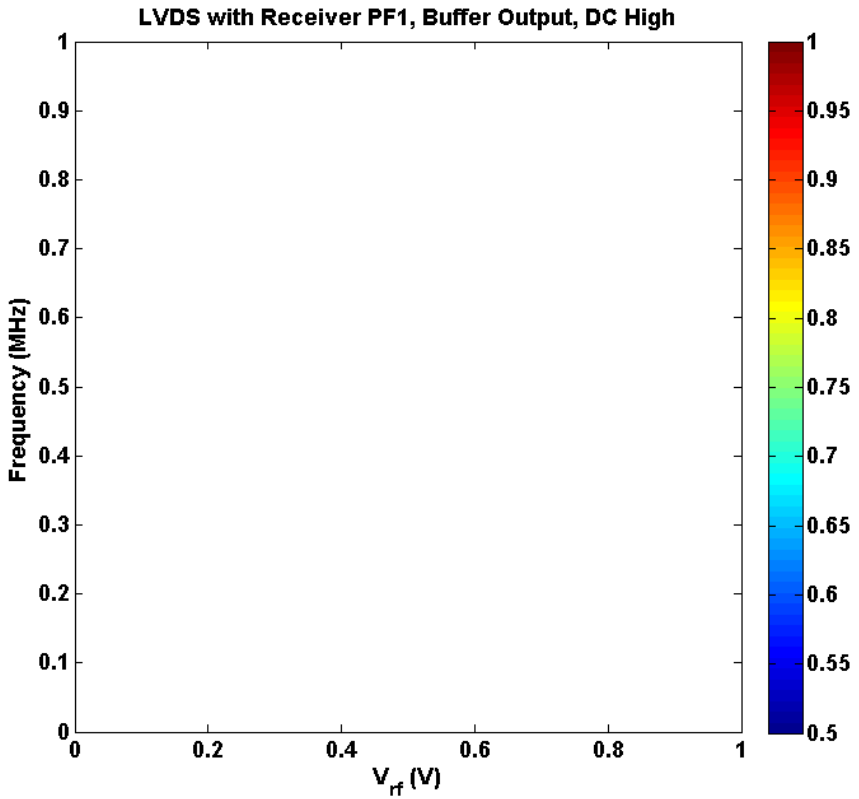




New comparator design introduces errors in the low-state, however… *(see next slide)*

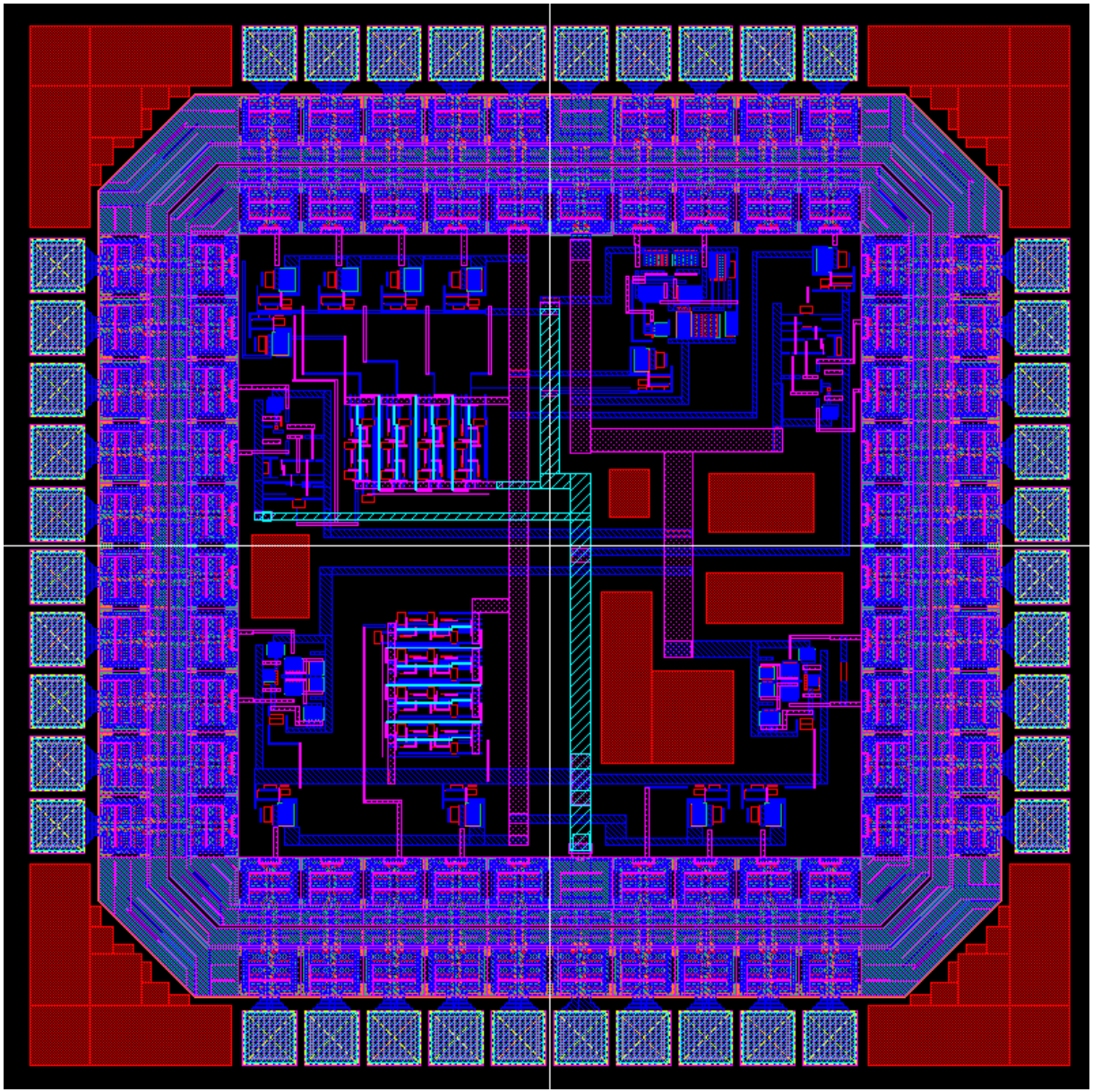
Mitigation II: Rethinking the Receiver





…however it cleans up the errors in the high-state within the same range.

Mitigation Example: Updated Receiver Chip



Summary of Experiments and Results

Test	Description	Rough Vulnerability Limits	Comments
In-House Design LVDS (Generation 1)	Standard LVDS implementation	Input LOW: -20 dBm for 200 to 300 MHz, -15 dBM for 300 to 500 MHz, changing between -20 to -15 between 500 MHz to 1 GHz Input HIGH: -7 dBm between 800 MHz and 1 GHz	
In-House Design SE (Generation 2)	Using single-ended signaling with buffers as TX&RX	Input LOW: -17 dBm for 200 to 300 MHz, no other error Input HIGH: -15 dBm below 100 MHz and above 300 MHz	
Commercial LVDS System, Type 1	COTS part	Input LOW: -7 dBm for 200 to 300 MHz, -5 dBm for 300 to 500 MHz, no other error Input HIGH: -5 dBM between 100 to 300 MHz, no other error	Difference between these commercial LVDS systems partly due to different ESD protection system architectures. (See input-pin IV measurements above.)
Commercial LVDS System, Type 2	COTS part	Input LOW: -7 dBm for below 200 MHz, changing between -20 to -13 dBm between 200 MHz to 1 GHz Input HIGH: Error between -20 to -10 dBm below 600 MHz	We are further analyzing HPM effects on the biasing of the transmitter circuit design to explain and mitigate the higher vulnerability of the in-house LVDS system.
Commercial SE System, Type 1	COTS part	Input LOW: No errors observed Input HIGH: -20 dBm between 100 and 600 MHz, -15 dBm from 600 to 800 MHz, -10 dBm from 800 MHz to 1 GHz	The commercial SE systems are more vulnerable in the high state.
Commercial SE System, Type 2	COTS part	Input LOW: No errors observed Input HIGH: -15 dBm from 100 to 600 MHz, -13 dBm from 600 to 800 MHz, -10 dBm from 800 MHz to 1 GHz	We are exploring difference between ESD structures, as well as HPM effects on the LVDS transmitter output stage, to understand the low-state differences better.
In-House Design DS System (Generation 2), Type 1: DDS	High-voltage differential signaling, using full digital signal amplitude	Simulation, compared to Gen1 LVDS circuit simulations Input LOW: No errors observed Input HIGH: The error limits shift to higher power and frequency HPM	There is a tradeoff between signal voltage levels (therefore power consumption) and HPM vulnerability. This circuit has been fabricated and is currently under test.
In-House Design (Generation 2), Type 2: New Receiver	Higher common-mode-rejection-ratio design for the receiver	Simulation, compared to Gen1 LVDS circuit used with Gen1 receiver design Input LOW: Introduces errors in the low-state for high excitation power and frequency above 250 MHz Input HIGH: Completely removes errors observed with the old design	Introducing an internal feedback architecture to improve common-mode-rejection-ratio of the receiver results in lower vulnerability overall. This circuit has been fabricated and is currently under test.

equipment needed to fabricate high quality SiN devices. The combined expertise of these two groups, along with the state-of-the-art facilities available at the University of Maryland provide this project with a strong chance of success.

Summary of Results: In this work, we have numerically and experimentally studied the response of modern CMOS ESD protection devices to HPM excitation. Our experimental results from circuits protected from electrostatic discharge by the ggNMOS/gcPMOS configuration reveal that the PN junctions between the drains and bodies of the ESD protection devices act in a manner similar to RF detectors for the incoming HPM excitation, introducing DC shifts at the input of the digital circuit. If the HPM frequency is relatively low, the gcPMOS response time can match that of the ggNMOS response, and the detection effects of both devices balance each other to limit the DC shift to around $V_{dd}/2$. At high frequencies, the PN junctions enter the NQS regime, where the transient response timescale of the junction potential becomes comparable to the period of the HPM signal. We have calculated that due to the difference between the NMOS and PMOS minority carrier mobilities, the gcPMOS will enter NQS operation nearly an octave lower in frequency compared to the ggNMOS. This creates a frequency range within which HPM signals can drive DC input responses to levels exceeding $V_{dd}/2$, possibly biasing the device at the undefined states between noise margins and causing unstable operation. For the process technology used in this work, we have experimentally and numerically established that this region falls between 600 MHz and 3 GHz. The frequency band will scale with CMOS process technologies; however in Section II we show that the device response can be calculated using process-specific device parameters and established semiconductor physics. Our analysis shows that the difference in the diffusion of minority carriers in the channels in the body region, which governs the diode transients, is responsible for the imbalance between the transient responses of the gcPMOS and ggNMOS. To model this effect, we used a simple but effective simulation technique to emulate the NQS behavior of the ESD protection devices for steady state, large-signal sinusoidal excitation. This technique involved using a substrate resistor network model provided as an option in BSIM4. This effectively places a resistance network between the drain-body PN junction and the source and body contacts. This network creates a time constant with the junction capacitance of the drain-body diode, which imitates the transition time of the reverse recovery process of the PN junction. This technique has allowed us to simulate the responses of the ESD protection circuits to obtain a better agreement with measurements. In simulating the response to HPM excitation across a wide frequency range, we have found that we also have to take into account and include the parasitic effects of the measurement setup, board traces, and package connections in the simulation by means of measured S-parameters. This combined method has allowed us to show good agreement with experimental results and highlights the aspects of the BSIM model which could be expanded in order to improve the HPM effects prediction capabilities in CMOS simulations, namely, the diffusion capacitance and the non-quasi-static behavior for the forward-biased drain/body diode.

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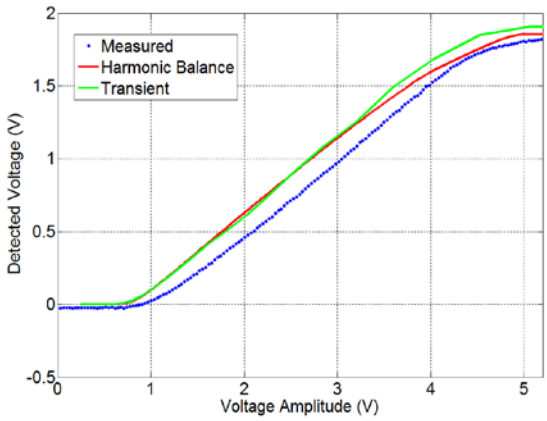

Fig. 17. Comparison of the measurements of the detected DC response at the excitation frequency of 2.5 GHz with simulation. The substrate resistance network was included with the BSIM parameters for these simulations.

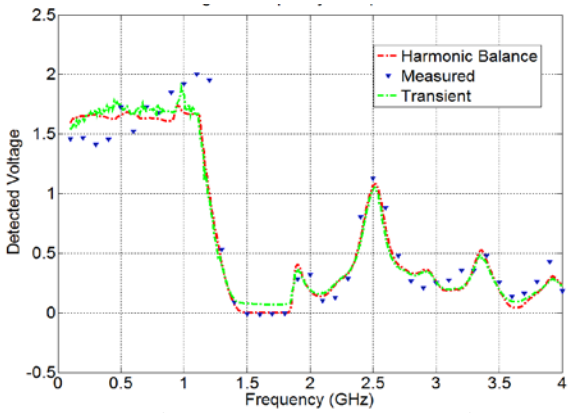

Fig. 18. Comparison of simulation with measurements of the detected DC voltage for a constant input power. The simulation accounts for parasitic elements of the measurement system, as well as the NQS diode transients.

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